HomePlug® 1.0 with Turbo
85 Mbps PHY

TECHNICAL DATA SHEET

INT5500

Intellon Turbo Powerline IC

Features

- Single-chip powerline networking transceiver with integrated MII interface
- Up to 85 Mbps data rate on the powerline
- Direct connection to Intellon INT1200 Analog Front End IC
- HomePlug 1.0 compatible
- Supports QAM 256/64/16, DQPSK, DBPSK and ROBO modulation schemes
- Multi-vendor flash compatibility
- Low power consumption
- Orthogonal Frequency Division Multiplexing (OFDM) with patented signal processing techniques for high data reliability in noisy media conditions
- Intelligent channel adaptation maximizes throughput under harsh channel conditions
- Integrated Quality of Service (QoS) features such as prioritized random access, contention-free access, and segment bursting
- 56-bit DES Link Encryption with key management for secure powerline communications
- In-circuit initialization of Flash memory via host interface
- “Boot From Host” and “Field-Upgradeable Firmware” features
- 1.8V core, 3.3V I/O Signaling
- 100-pin LQFP small footprint package

Applications

- Standard Video TV (SDTV) Distribution
- TV over IP (IPTV)
- Higher data rate broadband sharing
- Shared broadband internet access
- Audio and video streaming and transfer
- Expanding the coverage of wireless LANs
- Voice Over IP calls
- PC file and application sharing
- Printer and peripheral sharing
- Network and online gaming
- Security cameras

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1. General Description

The INT5500 IC is an integrated powerline MAC/PHY providing *No New Wires®* communications to any room, over any wire, at speeds of up to 85 Mbps. The INT5500 provides two interface options, selected via the Mode pin on the device:

- **INT5500 (PHY Option):** An MII PHY (IEEE 802.3u 1995, Paragraph 22) interface for interconnection to microcontrollers or Ethernet controllers. The INT5500 (PHY Option) is selected by strapping ASC_DATA/ Mode pin (pin 3) to VDD_IO through a 3.3KΩ resistor.

- **INT5500 (Host/DTE Option):** An MII Host/DTE interface (IEEE 802.3u 1995, Paragraph 22) for interconnection to an Ethernet PHY. The INT5500 (Host/DTE Option) is selected by connecting ASC_DATA/ Mode pin (pin 3) to VSS (GND) through a 3.3KΩ resistor.

The INT5500 Turbo powerline IC implements Intellon's patented technology and is fully compatible with the *HomePlug 1.0 Specification*. Specifically tailored to reliably deliver up to 85 Mbps over the difficult powerline communication environment, the IC combats deep attenuation notches, noise sources, and multi-path fading by allocating usable frequencies according to the signal to noise ratio (SNR). Synchronization is achieved in low SNR channels without the use of pilot carriers. Inclusion of additional modulation schemes increases the chipset's capability to attain higher throughput performance. The MAC implements a CSMA/CA protocol with prioritization and automatic repeat request (ARQ) for reliable delivery of Ethernet packets via packet encapsulation.

Built-in Quality of Service (QoS) features provide the necessary bandwidth for multimedia payloads including voice, data, audio, and video. A four-level prioritized random access method exists with strict adherence to priority. Segment bursting on the powerline minimizes the demands on the receiver resources and maximizes the throughput of the network while still providing excellent latency response and jitter performance. The IC's contention-free access capability extends this concept of segment bursting to allow the transmission of multiple frames over the powerline without relinquishing the control of the medium.

The INT5500 operates on 1.8V core and 3.3V I/O power, and is packaged in a 100-pin LQFP. Intellon offers a complete solution for powerline communication applications by providing the INT5500 in conjunction with the INT1200 Analog Front End IC.

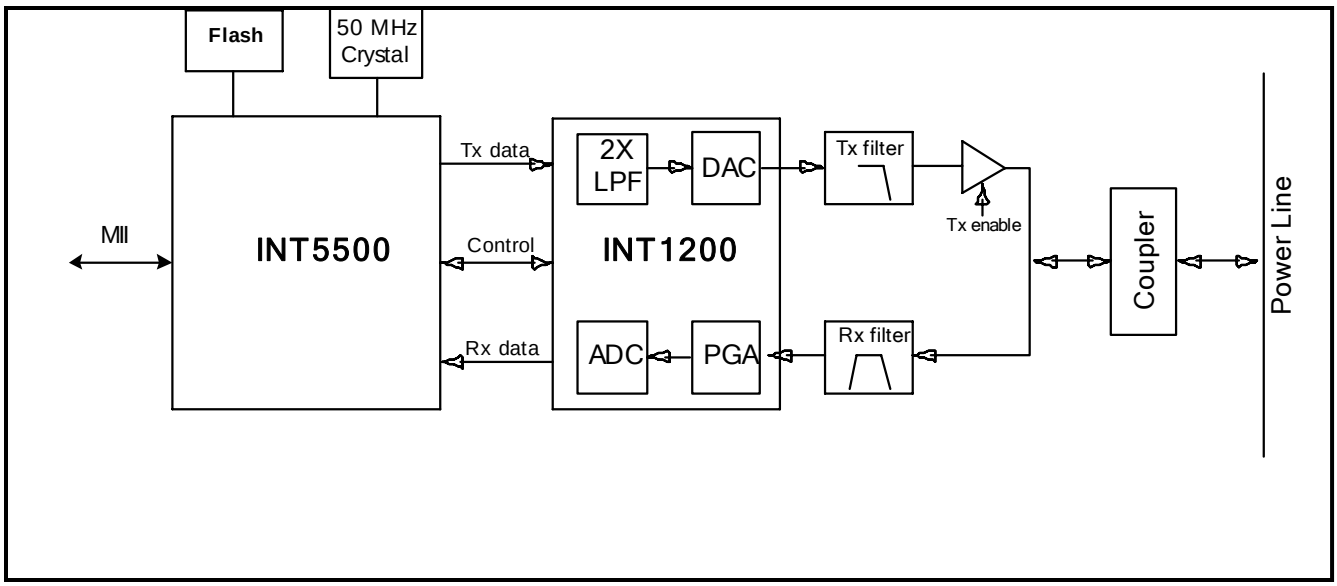


Figure 1: A General System Block Diagram of an INT5500CS based Powerline Device

2. Block Diagram

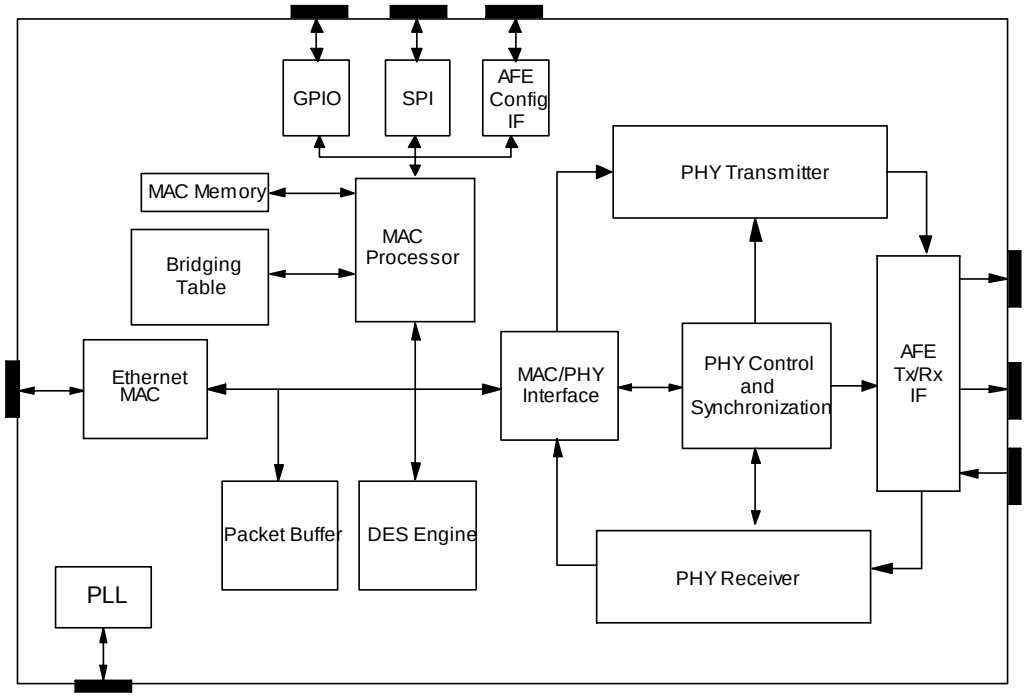


Figure 2: INT5500 IC Block Diagram

3. Master Pin Diagram

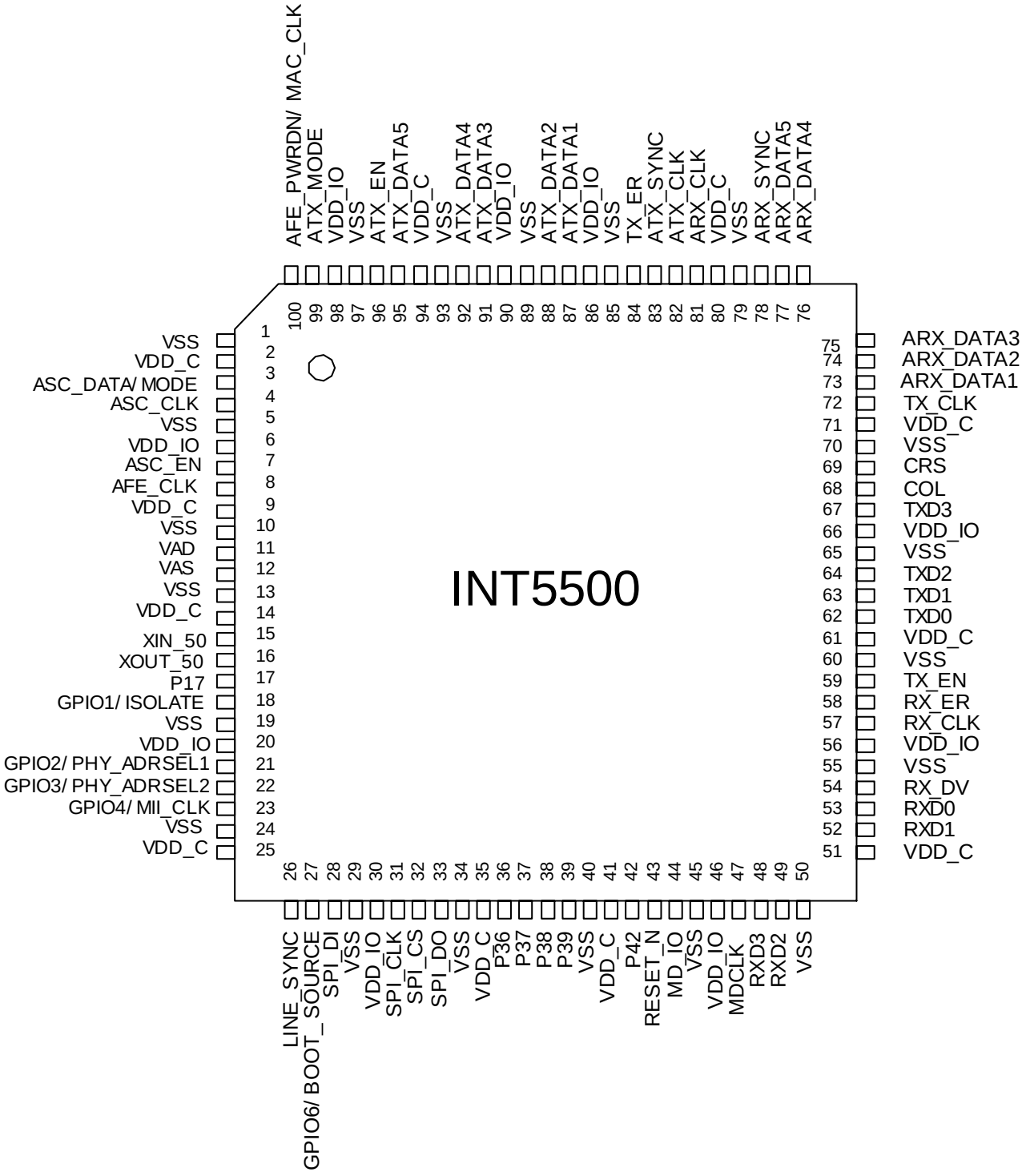


Figure 3: INT5500 IC Master Pin Diagram

4. Master Pin I/O

Pin No.	Signal	Pin No.	Signal
1	**VSS**	51	**VDD_C**
2	**VDD_C**	52	**RXD1**
3	**ASC_DATA/** MODE	53	**RXD0**
4	**ASC_CLK**	54	**RX_DV**
5	**VSS**	55	**VSS**
6	**VDD_IO**	56	**VDD_IO**
7	**ASC_EN**	57	**RX_CLK**
8	**AFE_CLK**	58	**RX_ER**
9	**VDD_C**	59	**TX_EN**
10	**VSS**	60	**VSS**
11	**VAD**	61	**VDD_C**
12	**VAS**	62	**TXD0**
13	**VSS**	63	**TXD1**
14	**VDD_C**	64	**TXD2**
15	**XIN_50**	65	**VSS**
16	**XOUT_50**	66	**VDD_IO**
17	**P17**	67	**TXD3**
18	**GPIO1/** ISOLATE	68	**COL**
19	**VSS**	69	**CRS**
20	**VDD_IO**	70	**VSS**
21	**GPIO2/** PHY_ADRSEL1	71	**VDD_C**
22	**GPIO3/** PHY_ADRSEL2	72	**TX_CLK**
23	**GPIO4/** MII_CLK	73	**ARX_DATA1**
24	**VSS**	74	**ARX_DATA2**
25	**VDD_C**	75	**ARX_DATA3**
26	**LINE_SYNC**	76	**ARX_DATA4**
27	**GPIO6/** BOOT_SOURCE	77	**ARX_DATA5**
28	**SPI_DI**	78	**ARX_SYNC**
29	**VSS**	79	**VSS**
30	**VDD_IO**	80	**VDD_C**
31	**SPI_CLK**	81	**ARX_CLK**
32	**SPI_CS**	82	**ATX_CLK**
33	**SPI_DO**	83	**ATX_SYNC**
34	**VSS**	84	**TX_ER**
35	**VDD_C**	85	**VSS**
36	**P36**	86	**VDD_IO**
37	**P37**	87	**ATX_DATA1**
38	**P38**	88	**ATX_DATA2**
39	**P39**	89	**VSS**
40	**VSS**	90	**VDD_IO**
41	**VDD_C**	91	**ATX_DATA3**
42	**P42**	92	**ATX_DATA4**
43	**RESET_N**	93	**VSS**
44	**MD_IO**	94	**VDD_C**
45	**VSS**	95	**ATX_DATA5**
46	**VDD_IO**	96	**ATX_EN**
47	**MDCLK**	97	**VSS**
48	**RXD3**	98	**VDD_IO**
49	**RXD2**	99	**ATX_MODE**
50	**VSS**	100	**AFE_PWRDN/** MAC_CLK

5. Pin Description

Pin No.	Signal	Description
1	**VSS**	Ground
2	**VDD_C**	1.8V Core Supply Voltage
3	**ASC_DATA/** MODE	AFE Serial Interface Data The pull-up/ pull-down value is latched as MODE input during power up/ reset. Refer section 7.2 for more details.
4	**ASC_CLK**	AFE serial interface clock. This pin must be pulled low at power-up/reset.
5	**VSS**	Ground
6	**VDD_IO**	3.3V I/O Supply Voltage
7	**ASC_EN**	Active low AFE serial interface strobe. This pin to be pulled low during power up/ reset.
8	**AFE_CLK**	25 MHz clock reference to AFE.
9	**VDD_C**	1.8V Core Supply Voltage
10	**VSS**	Ground
11	**VAD**	PLL VDD (1.8 V). Refer to section 7.5 for more details.
12	**VAS**	PLL VSS (ground). Refer to section 7.5 for more details.
13	**VSS**	Ground
14	**VDD_C**	1.8V Core Supply Voltage
15	**XIN_50**	50 MHz clock logic signal input or crystal connection.
16	**XOUT_50**	50 MHz clock crystal connection (when using built-in oscillator).
17	**P17**	Connect to VSS through a 3.3KΩ resistor
18	**GPIO1/** ISOLATE	General-Purpose Input/Output 1. The pull-up/ pull-down value is latched as MII ISOLATE input INT5500 PHY mode during power up/ reset. Refer section 7.2 for more details.
19	**VSS**	Ground
20	**VDD_IO**	3.3V I/O Supply Voltage
21	**GPIO2/** PHY_ADRSEL1	General-Purpose Input/Output 2. The pull-up/ pull-down value is latched as PHY Address Select input during power up/ reset in the INT5500 PHY mode. Refer section 7.2 for more details.
22	**GPIO3/** PHY_ADRSEL2	General-Purpose Input/Output 3. The pull-up/ pull-down value is latched as PHY Address Select input during power up/ reset in the INT5500 PHY mode. Refer section 7.2 for more details.
23	**GPIO4/** MII_CLK	General-Purpose Input/Output 4. The pull-up/ pull-down value is latched to select MII clock speed in INT5500 PHY mode during power up/ reset. Refer section 7.2 for more details.
24	**VSS**	Ground
25	**VDD_C**	1.8V Core Supply Voltage
26	**LINE_SYNC**	Line Sync
27	**GPIO6/** BOOT_ SOURCE	General-Purpose Input/Output 6. The pull-up/ pull-down value is latched as Boot Source input during power up/ reset. Refer section 7.2 for more details.
28	**SPI_DI**	Non-Volatile Memory SPI interface data input.
29	**VSS**	Ground
30	**VDD_IO**	3.3V I/O Supply Voltage
31	**SPI_CLK**	Non-Volatile Memory SPI interface clock.

Pin No.	Signal	Description
32	**SPI_CS**	Non-Volatile Memory SPI interface chips select (active low).
33	**SPI_DO**	Non-Volatile Memory SPI interface data out.
34	**VSS**	Ground
35	**VDD_C**	1.8V Core Supply Voltage
36	**P36**	Connect to VDD_IO through a 3.3KΩ resistor.
37	**P37**	Connect to VSS through a 3.3KΩ resistor
38	**P38**	Connect to VDD_IO through a 3.3KΩ resistor
39	**P39**	Connect to VDD_IO through a 3.3KΩ resistor
40	**VSS**	Ground
41	**VDD_C**	1.8V Core Supply Voltage
42	**P42**	Connect to VDD_IO through a 3.3KΩ resistor
43	**RESET_N**	Reset Input. Resets all IC logic when low.
44	**MD_IO**	MII Management Data Input/Output
45	**VSS**	Ground
46	**VDD_IO**	3.3V I/O Supply Voltage
47	**MDCLK**	MII Management Data Clock
48	**RXD3**	MII RX Data bit 3
49	**RXD2**	MII RX Data bit 2
50	**VSS**	Ground
51	**VDD_C**	1.8V Core Supply Voltage
52	**RXD1**	MII RX Data bit 1
53	**RXD0**	MII RX Data bit 0
54	**RX_DV**	MII RX Data Valid
55	**VSS**	Ground
56	**VDD_IO**	3.3V I/O Supply Voltage
57	**RX_CLK**	MII RX Clock
58	**RX_ER**	MII RX Error
59	**TX_EN**	MII TX Enable
60	**VSS**	Ground
61	**VDD_C**	1.8V Core Supply Voltage
62	**TXD0**	MII TX data bit 0
63	**TXD1**	MII TX data bit 1
64	**TXD2**	MII TX data bit 2
65	**VSS**	Ground
66	**VDD_IO**	3.3V I/O Supply Voltage
67	**TXD3**	MII TX data bit 3
68	**COL**	MII Collision Detect
69	**CRS**	MII Carrier Sense
70	**VSS**	Ground
71	**VDD_C**	1.8V Core Supply Voltage
72	**TX_CLK**	MII TX Clock
73	**ARX_DATA1**	AFE receive data. Data is received from the AFE on this bus synchronous to ARX_CLK with upper/lower nibble framed by ARX_SYNC. This is a time division-multiplexed data bus that carries 10-bit received data in two nibbles of 5 bits each. The receive data rate is 50 MSPS giving a nibble rate of 100 MHz
74	**ARX_DATA2**	
75	**ARX_DATA3**	
76	**ARX_DATA4**	
77	**ARX_DATA5**	
78	**ARX_SYNC**	AFE receive data synchronization strobe. Low: indicates that the MS nibble of the data is present on ARX_DATA []. High: indicates that the LS nibble of the data is present on ARX_DATA []. For every word that passes across the interface, the MS nibble always appears first followed by the LS nibble second.
79	**VSS**	Ground
80	**VDD_C**	1.8V Core Supply Voltage
81	**ARX_CLK**	AFE receive data clock (100 MHz). Note that this pin is not 5 V-tolerant

Pin No.	Signal	Description
82	**ATX_CLK**	AFE transmit data clock (100 MHz). Note that this pin is not 5 V-tolerant
83	**ATX_SYNC**	AFE transmit data synchronization strobe. Low: indicates that the MS nibble is present on the ATX_DATA [] bus. High: indicates that the LS nibble is present on the ATX_DATA [] bus. For every word that passes across the interface, the MS nibble always appears first followed by the LS nibble second. Note: ATX_SYNC remains low while ATX_MODE is asserted as gain data is not multiplexed
84	**TX_ER**	MII transmit data error.
85	**VSS**	Ground
86	**VDD_IO**	3.3V I/O Supply Voltage
87	**ATX_DATA1**	AFE transmit data bus. This is a time division-multiplexed data bus that carries 10-bit transmit data in two nibbles of 5 bits each. The transmit rate is 50 MSPS giving a nibble rate of 100 MHz. While ATX_MODE is asserted, this bus carries 5-bit non-multiplexed gain data for the receive path.
88	**ATX_DATA2**	
91	**ATX_DATA3**	
92	**ATX_DATA4**	
95	**ATX_DATA5**	
89	**VSS**	Ground
90	**VDD_IO**	3.3V I/O Supply Voltage
93	**VSS**	Ground
94	**VDD_C**	1.8V Core Supply Voltage
96	**ATX_EN**	Transmit enable. Asserted: indicates that a transmission is in progress. Negated: indicates that a transmission is not in progress (receive mode).
97	**VSS**	Ground
98	**VDD_IO**	3.3V I/O Supply Voltage
99	**ATX_MODE**	AFE gain transmit data port mode.
100	**AFE_PWRDN/** MAC_CLK	AFE power down. The pull-up/ pull-down value is latched to select MAC Clock speed during power up/ reset. Refer section 7.2 for more details.

6. INT5500 System Overview

The INT5500 is set up in one of the two configurations: Host/DTE Mode and PHY Mode.

6.1. MII Host/DTE Mode

The INT5500 implements an MII interface as defined by the IEEE 802.3u. This interface comprises a data interface and a management interface. The data interface is used for exchanging data between the INT5500 and the 802.3u compliant MII PHY. The management interface allows the INT5500 to control and monitor the attached Ethernet PHY.

The MII data interface consists of separate 4-bit data paths for transmit and receive data along with carrier sense and collision detection. Data is transferred between the MAC and PHY over each 4-bit data path synchronous with a clock signal supplied to the INT5500 (Host/DTE Option) by the Ethernet PHY.

The MII management interface provides access to the status and control registers in the Ethernet PHY. Further details of the MII can be found in the IEEE 802.3u Standard.

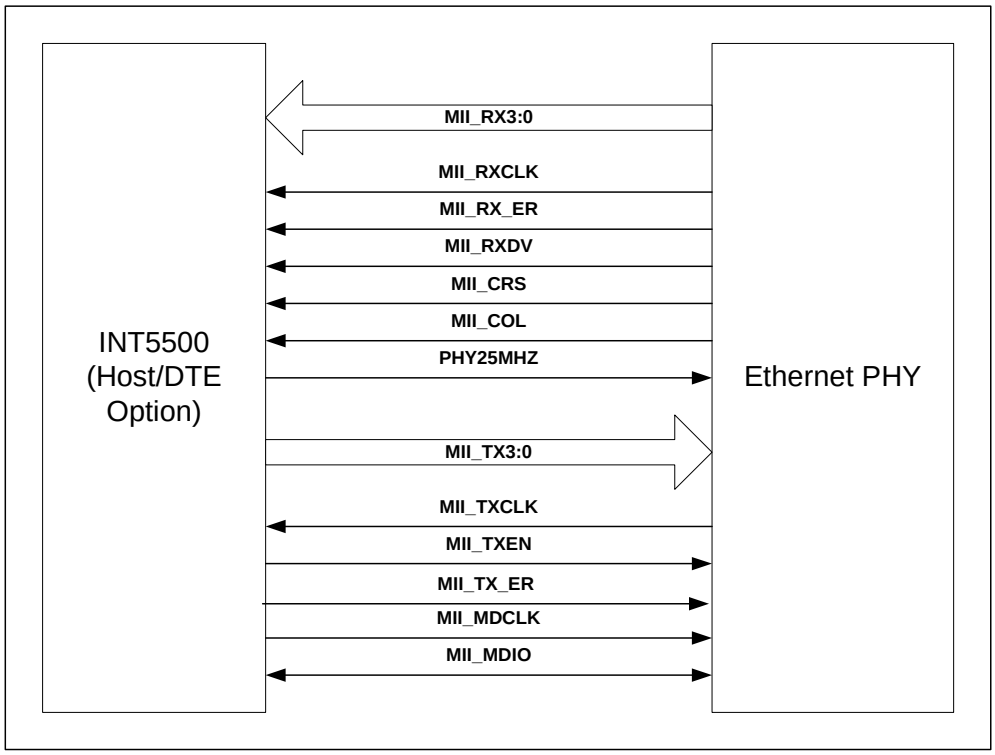


Figure 4: MII Interface to INT5500 (Host/DTE Option)

6.2. MII PHY Mode

MII is an industry standard, multi vendor, interoperable interface between the MAC and PHY sub-layers. It provides a simple interconnection between the INT5500 and IEEE 802.3u Ethernet MAC controllers from a variety of sources. The MII consists of separate 4-bit data paths for transmit and receive data along with carrier sense and collision detection. Data is transferred between the MAC and PHY over each 4-bit data path synchronous with a clock signal supplied to the MAC by the INT5500. The MII interface also provides a two-wire bi-directional serial management data interface. This interface provides access to the status and control registers in the INT5500. Further details of the MII can be found in the IEEE 802.3u Standard.

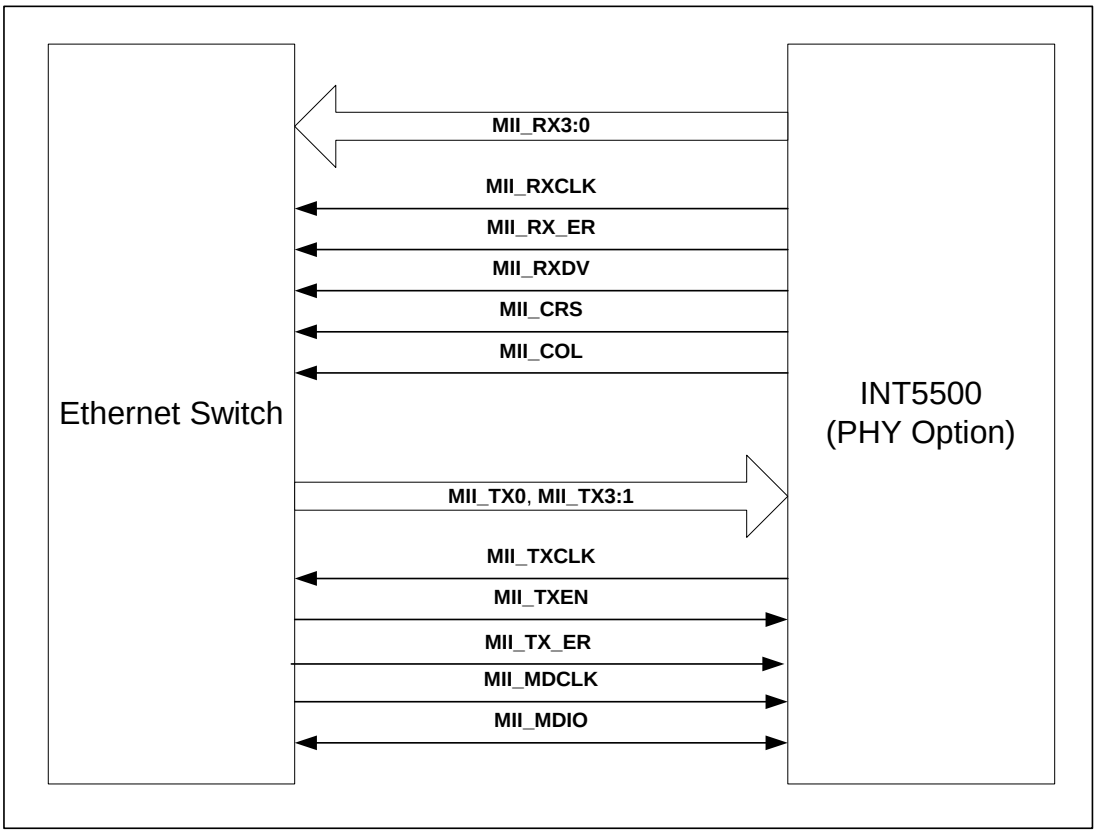


Figure 5: MII Interface to INT5500 (PHY Option)

6.3. Pin Assignment in Different INT5500 Mode

Pin No.	Signal	PHY Mode (I/O) *PHY mode is selected by connecting the ASC_DATA/ MODE (pin3) to VDD_IO through a 3.3KΩ resistor*	Host/ DTE Mode (I/O) *Host/ DTE mode is selected by connecting the ASC_DATA/ MODE (pin3) to VSS through a 3.3KΩ resistor*
1	**VSS**	Ground (I)	Ground (I)
2	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
3	**ASC_DATA/** MODE	AFE Serial Interface Data. (I/O) The pull-up/ pull-down value is latched as MODE during power up/ reset. PHY mode is selected by connecting the ASC_DATA/ MODE (pin3) to VDD_IO through a 3.3KΩ resistor	AFE Serial Interface Data (I/O) The pull-up/ pull-down value is latched as MODE during power up/ reset. Host/ DTE mode is selected by connecting the ASC_DATA/ MODE (pin3) to VSS through a 3.3KΩ resistor
4	**ASC_CLK**	AFE serial interface clock. (O) This pin must be pulled low.	AFE serial interface clock (O) This pin must be pulled low.
5	**VSS**	Ground (I)	Ground (I)
6	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)
7	**ASC_EN**	Active low AFE serial interface strobe (O).	Active low AFE serial interface strobe (O).
8	**AFE_CLK**	25 MHz clock reference to AFE (O).	25 MHz clock reference to AFE (O).
9	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
10	**VSS**	Ground (I)	Ground (I)
11	**VAD**	PLL VDD (1.8 V). Refer to section 7.5 for more details	PLL VDD (1.8 V). Refer to section 7.5 for more details
12	**VAS**	PLL VSS (ground). Refer to section 7.5 for more details	PLL VSS (ground). Refer to section 7.5 for more details
13	**VSS**	Ground (I)	Ground (I)
14	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
15	**XIN_50**	50 MHz clock logic signal input or crystal connection (I).	50 MHz clock logic signal input or crystal connection (I).
16	**XOUT_50**	50 MHz clock crystal connection (when using built-in oscillator) (O).	50 MHz clock crystal connection (O)
17	**P17**	Connect to VSS through a 3.3KΩ resistor	Connect to VSS through a 3.3KΩ resistor
18	**GPIO1/** ISOLATE	General-Purpose Input/Output 1 (I/O) The pull-up/ pull-down value is latched as MII ISOLATE input during power up/ reset. Refer section 7.2 for more details.	General-Purpose Input/Output 1 (I/O). This pin shall be tied LOW during power up/ reset.
19	**VSS**	Ground (I)	Ground (I)
20	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)
21	**GPIO2/** PHY_ADRSEL1	General-Purpose Input/Output 2 (I/O). The pull-up/ pull-down value is latched as PHY Address Select input during power up/ reset in the INT5500 PHY mode. Refer section 7.2 for more details	General-Purpose Input/Output 2 (I/O). This pin shall be tied HIGH during power up/ reset.
22	**GPIO3/** PHY_ADRSEL2	General-Purpose Input/Output 3 (I/O). The pull-up/ pull-down value is latched as PHY Address Select input during power up/ reset in the INT5500 PHY mode. Refer section 7.2 for more details	General-Purpose Input/Output 3 (I/O). This pin shall be tied LOW during power up/ reset.
23	**GPIO4/** MII_CLK	General-Purpose Input/Output 4 (I/O) The pull-up/ pull-down value is latched to select MII clock speed in INT5500 PHY mode during power up/ reset. Refer section 7.2 for more	General-Purpose Input/Output 4 (I/O). This pin should be tied HIGH during power up/ reset.

Pin No.	Signal	PHY Mode (I/O) *PHY mode is selected by connecting the ASC_DATA/ MODE (pin3) to VDD_IO through a 3.3KΩ resistor*	Host/ DTE Mode (I/O) *Host/ DTE mode is selected by connecting the ASC_DATA/ MODE (pin3) to VSS through a 3.3KΩ resistor*
		details	
24	**VSS**	Ground	Ground
25	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
26	**LINE_SYNC**	Line Sync (I/O)	Line Sync (I/O)
27	**GPIO6/** BOOT_SOURCE	General-Purpose Input/Output 6 (I/O). The pull-up/ pull-down value is latched as Boot Source input during power up/ reset. Refer section 7.2 for more details.	General-Purpose Input/Output 6 (I/O). The pull-up/ pull-down value is latched as Boot Source input during power up/ reset. Refer section 7.2 for more details.
28	**SPI_DI**	Non-Volatile Memory SPI interface data input (I).	Non-Volatile Memory SPI interface data input (I).
29	**VSS**	Ground (I)	Ground (I)
30	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)
31	**SPI_CLK**	Non-Volatile Memory SPI interface clock (O).	Non-Volatile Memory SPI interface clock (O).
32	**SPI_CS**	Non-Volatile Memory SPI interface chips select (active low) (O).	Non-Volatile Memory SPI interface chips select (active low) (O).
33	**SPI_DO**	Non-Volatile Memory SPI interface data out (O).	Non-Volatile Memory SPI interface data out (O).
34	**VSS**	Ground (I)	Ground (I)
35	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
36	**P36**	Connect to VDD_IO through a 3.3KΩ resistor (I).	Connect to VDD_IO through a 3.3KΩ resistor (I).
37	**P37**	Connect to VSS through a 3.3KΩ resistor (I)	Connect to VSS through a 3.3KΩ resistor (I)
38	**P38**	Connect to VDD_IO through a 3.3KΩ resistor (I)	Connect to VDD_IO through a 3.3KΩ resistor (I)
39	**P39**	Connect to VDD_IO through a 3.3KΩ resistor (I)	Connect to VDD_IO through a 3.3KΩ resistor (I)
40	**VSS**	Ground (I)	Ground (I)
41	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
42	**P42**	Connect to VDD_IO through a 3.3KΩ resistor (O)	Connect to VDD_IO through a 3.3KΩ resistor (O)
43	**RESET_N**	Reset Input. Resets all IC logic when low (I).	Reset Input. Resets all IC logic when low (I).
44	**MD_IO**	MII Management Data Input/Output (I/0)	MII Management Data Input/Output (I/0)
45	**VSS**	Ground (I)	Ground (I)
46	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)
47	**MDCLK**	MII Management Data Clock (I) The MDCLK signal is a clock reference for the MD_IO signal.	MII Management Data Clock (O) The MDCLK signal is a clock reference for the MD_IO signal.
48	**RXD3**	MII RX Data (O) Data is transferred from the IC across these four lines one nibble at a time	MII RX Data (I) Data is transferred from the IC across these four lines one nibble at a time.
49	**RXD2**		
52	**RXD1**		
53	**RXD0**		
50	**VSS**	Ground (I)	Ground (I)
51	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
54	**RX_DV**	MII RX Data Valid (O) This Signal indicates that the data on the RXD [3:0] pins are valid	MII RX Data Valid (I) This Signal indicates that the data on the RXD [3:0] pins are valid.
55	**VSS**	Ground (I)	Ground (I)
56	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)

Pin No.	Signal	PHY Mode (I/O) *PHY mode is selected by connecting the ASC_DATA/ MODE (pin3) to VDD_IO through a 3.3KΩ resistor*	Host/ DTE Mode (I/O) *Host/ DTE mode is selected by connecting the ASC_DATA/ MODE (pin3) to VSS through a 3.3KΩ resistor*
57	**RX_CLK**	MII RX Clock (O) The RX Clock is synchronous to the data and is continuous.	MII RX Clock (I) The RX Clock is synchronous to the incoming data and is continuous. This clock operates at 25 MHz (100BaseT) or 2.5MHz (10BaseT).
58	**RX_ER**	MII RX Error (O) The RX_ER signal indicates that an error has occurred during frame reception	MII RX Error (I) The RX_ER signal indicates that an error has occurred during frame reception
59	**TX_EN**	MII TX Enable (I) The MII TX Enable signal indicates that valid data is present on the TXD [3:0] pins.	MII TX Enable (O) The MII TX Enable signal indicates that valid data is present on the TXD [3:0] pins.
60	**VSS**	Ground (I)	Ground (I)
61	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
62	**TXD0**	MII TX data (I) Data is transferred to the IC across the four lines one nibble at a time.	MII TX data (O) Data is transferred to the IC across the four lines one nibble at a time.
63	**TXD1**		
64	**TXD2**		
67	**TXD3**		
65	**VSS**	Ground (I)	Ground (I)
66	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)
68	**COL**	MII Collision Detect (O) The MII Collision Detect Signal indicates to the MAC that a collision has occurred on the MII interface. MII_COL is an asynchronous output signal.	MII Collision Detect (I) The MII Collision Detect Signal indicates to the MAC that a collision has occurred on the MII interface and shall remain asserted while the collision condition persists.
69	**CRS**	MII Carrier Sense (O) The MII Carrier Sense signal is asserted within 30 MII clocks after TX_EN indicates a TX frame is being sent by the local host. MII CRS stays true until the entire TX frame is loaded into an internal buffer AND a new buffer is allocated to the MII TX interface. This signal should be used monitored by the MII TX host. A new MII TX frame should not be sent until MII CRS returns to false to prevent TX buffer overflows. CRS is an asynchronous output signal.	MII Carrier Sense (I) The MII Carrier Sense signal is asserted when either the TX or RX medium is non-idle.
70	**VSS**	Ground (I)	Ground (I)
71	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
72	**TX_CLK**	MII TX Clock (O) The TX Clock outputs a continuous clock. This clock operates at 25MHz	MII TX Clock (I) The TX Clock is a continuous clock into the INT5500. This clock operates at 25MHz(100BaseT) or 2.5MHz(10BaseT)
73	**ARX_DATA1**	AFE receive data (I). Data are received from the AFE on this bus synchronous to ARX_CLK with upper/lower nibble framed by ARX_SYNC.	AFE receive data (I). Data are received from the AFE on this bus synchronous to ARX_CLK with upper/lower nibble framed by ARX_SYNC. This is a time
74	**ARX_DATA2**		
75	**ARX_DATA3**		
76	**ARX_DATA4**		

Pin No.	Signal	PHY Mode (I/O) *PHY mode is selected by connecting the ASC_DATA/ MODE (pin3) to VDD_IO through a 3.3KΩ resistor*	Host/ DTE Mode (I/O) *Host/ DTE mode is selected by connecting the ASC_DATA/ MODE (pin3) to VSS through a 3.3KΩ resistor*
77	**ARX_DATA5**	This is a time division-multiplexed data bus that carries 10-bit received data in two nibbles of 5 bits each. The receive data rate is 50 MSPS giving a nibble rate of 100 MHz	division-multiplexed data bus that carries 10-bit received data in two nibbles of 5 bits each. The receive data rate is 50 MSPS giving a nibble rate of 100 MHz
78	**ARX_SYNC**	AFE receive data synchronization strobe (I). Low: indicates that the MS nibble of the data is present on ARX_DATA []. High: indicates that the LS nibble of the data is present on ARX_DATA []. For every word that passes across the interface, the MS nibble always appears first followed by the LS nibble second	AFE receive data synchronization strobe (I). Low: indicates that the MS nibble of the data is present on ARX_DATA []. High: indicates that the LS nibble of the data is present on ARX_DATA []. For every word that passes across the interface, the MS nibble always appears first followed by the LS nibble second
79	**VSS**	Ground (I)	Ground (I)
80	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
81	**ARX_CLK**	AFE receive data clock (100 MHz) (I). Note: This pin is not 5 V-tolerant	AFE receive data clock (100 MHz) (I). Note: This pin is not 5V-tolerant
82	**ATX_CLK**	AFE transmit data clock (100 MHz) (I). Note: This pin is not 5 V-tolerant	AFE transmit data clock (100 MHz) (I). Note: This pin is not 5 V-tolerant
83	**ATX_SYNC**	AFE transmit data synchronization strobe (O). Low: indicates that the MS nibble is present on the ATX_DATA [] bus. High: indicates that the LS nibble is present on the ATX_DATA [] bus. For every word that passes across the interface, the MS nibble always appears first followed by the LS nibble second. Note: ATX_SYNC remains low while ATX_MODE is asserted as gain data is not multiplexed	AFE transmit data synchronization strobe (O). Low: indicates that the MS nibble is present on the ATX_DATA [] bus. High: indicates that the LS nibble is present on the ATX_DATA [] bus. For every word that passes across the interface, the MS nibble always appears first followed by the LS nibble second. Note: ATX_SYNC remains low while ATX_MODE is asserted as gain data is not multiplexed
84	**TX_ER**	MII TX Error (I) Assertion of this signal causes intentionally bad data to be transmitted. The MII interface will discard any incoming frame received when and if this signal is asserted while TX_EN is true.	MII TX Error (O) Assertion of this signal causes intentionally bad data to be transmitted.
85	**VSS**	Ground (I)	Ground (I)
86	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)
87	**ATX_DATA1**	AFE transmit data bus (O). This is a time division-multiplexed data bus that carries 10-bit transmit data in two nibbles of 5 bits each. The transmit rate is	AFE transmit data bus (O). This is a time division-multiplexed data bus that carries 10-bit transmit data in two nibbles of 5 bits each. The transmit rate is 50 MSPS
88	**ATX_DATA2**		
91	**ATX_DATA3**		
92	**ATX_DATA4**		

Pin No.	Signal	PHY Mode (I/O) ***PHY mode is selected by connecting the ASC_DATA/ MODE (pin3) to VDD_IO through a 3.3KΩ resistor***	Host/ DTE Mode (I/O) ***Host/ DTE mode is selected by connecting the ASC_DATA/ MODE (pin3) to VSS through a 3.3KΩ resistor***
95	**ATX_DATA5**	50 MSPS giving a nibble rate of 100 MHz. While ATX_MODE is asserted, this bus carries 5-bit non-multiplexed gain data for the receive path.	giving a nibble rate of 100 MHz. While ATX_MODE is asserted, this bus carries 5-bit non-multiplexed gain data for the receive path.
89	**VSS**	Ground (I)	Ground (I)
90	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)
93	**VSS**	Ground (I)	Ground (I)
94	**VDD_C**	1.8V Core Supply Voltage (I)	1.8V Core Supply Voltage (I)
96	**ATX_EN**	Transmit enable (O). Asserted: indicates that a transmission is in progress. Negated: indicates that a transmission is not in progress (receive mode).	Transmit enable (O). Asserted: indicates that a transmission is in progress. Negated: indicates that a transmission is not in progress (receive mode).
97	**VSS**	Ground (I)	Ground (I)
98	**VDD_IO**	3.3V I/O Supply Voltage (I)	3.3V I/O Supply Voltage (I)
99	**ATX_MODE**	AFE gain transmit data port mode (O).	AFE gain transmit data port mode (O).
100	**AFE_PWRDN**	AFE power down (O). The pull-up/ pull-down value is latched to select MAC Clock speed during power up/ reset. Refer section 7.2 for more details.	AFE power down (O). The pull-up/ pull-down value is latched to select MAC Clock speed during power up/ reset. Refer section 7.2 for more details.

7. Design Considerations

7.1. MAC Firmware Boot Option

The INT5500 MAC Firmware can be initialized in two ways:

- **Boot from Flash:** The INT5500 IC provides a Serial Peripheral Interface (SPI) for downloading the run-time MAC software from an on-board flash memory device. The INT5500 acts as a master on the SPI. The Flash currently supported is the M25P10-A [1M] from STMicroelectronics. Refer to Section 7.2 for the required strapping options.

- **Boot from Host:** The INT5500 IC can be initialized from the host interface. Please refer to the Software Development Kit for initialization details.

7.2. INT5500 Configuration Straps

The INT5500 supports many configuration options. Most configuration options are selected through the firmware configuration block (refer to INT5500 SDK technical manual for more details). However, some configuration settings are available to hardware and boot software during and immediately following a power-on reset. These configuration parameters are controlled by strap settings that are read upon release from reset to determine the INT5500 state of several pins.

Attaching a pull-up or pull-down resistor, as appropriate, sets the state of the pins. Once the strap state has been read and the INT5500 has loaded the MAC firmware, each pin assumes its normal operation function.

Note: The value of the pull-up or pull-down resistors used to configure the straps must be 3.3K Ohms or lower.

Table 1 - Configuration Strapping Options (General)

Strap	Description	Value	Setting
ASC_EN	Reserved	Low	Must be set to low
ASC_DATA/MODE	Operation mode	Low	Host/DTE Mode
		High	PHY Mode
ASC_CLK	Reserved	Low	Must be set to Low
ASC_PWRDWN/MAC_CLK	Boot clock speed	Low	50 MHz (recommended)
		High	75 MHz
GPIO6	Boot source	Low	Boot from serial flash
		High	Boot from host

When the INT5500 is configured to boot from serial flash, the INT5500 will default to boot from host if no valid image is detected in the serial flash.

7.2.1. Host/DTE Mode Configuration Straps

In Host/DTE Mode, the GPIO pins shall be configured as shown below.

Table 2 - INT5500 Host/DTE Mode Strapping Options

Strap	Value	Setting
GPIO1	Low	Connect to Gnd
GPIO2	High	Connect to +3.3V
GPIO3	Low	Connect to Gnd
GPIO4	High	Connect to +3.3V

Note: All straps shall be configured to the desired setting through a 3.3KΩ Resistor or lower.

7.2.2. PHY Mode Configuration Straps

In PHY Mode, the INT5500 can load the MAC firmware from the serial flash or it may boot using the host interface. Table 3 lists the additional strapping options that configure the MII bus during power-up. The speed of the MII bus shall be set at power-on.

Table 3 – INT5500 PHY Mode Strapping Options

Strap	Description	Value	Setting
ISOLATE/ GPIO1	MII isolate state	Low	MII isolate off [default]
		High	MII isolate on
PHY_ADRSEL [1]/ GPIO2: **PHY_ADRSEL [2]**/GPIO3	MII PHY Address	Low: Low	0b00001
		High: Low	0b00010
		Low: High	0b00000
		High: High	0b00100
MII_CLK/ GPIO4	MII bus speed	Low	2.5 MHz (10 Mbps)
		High	25 MHz (100 Mbps)

7.3. INT5500 Clock Source

The INT5500 requires an external 50 MHz clock reference. This can be provided by a crystal oscillator circuit connected across its XIN_50 and XOUT_50 pins or by a logic clock signal applied to the XIN_50 input.

The INT5500 built-in PLL clock multiplier generates all required internal clocks from the master clock reference. A 25 MHz clock output (AFE_CLK) is provided as a clock reference for AFE and external PHY chipset. The INT1200 IC returns two 100 MHz clocks as references for the RX and TX data interfaces (ARX_CLK and ATX_CLK, respectively).

The recommended clocking arrangement for INT5500 based design is shown in Figure 6.

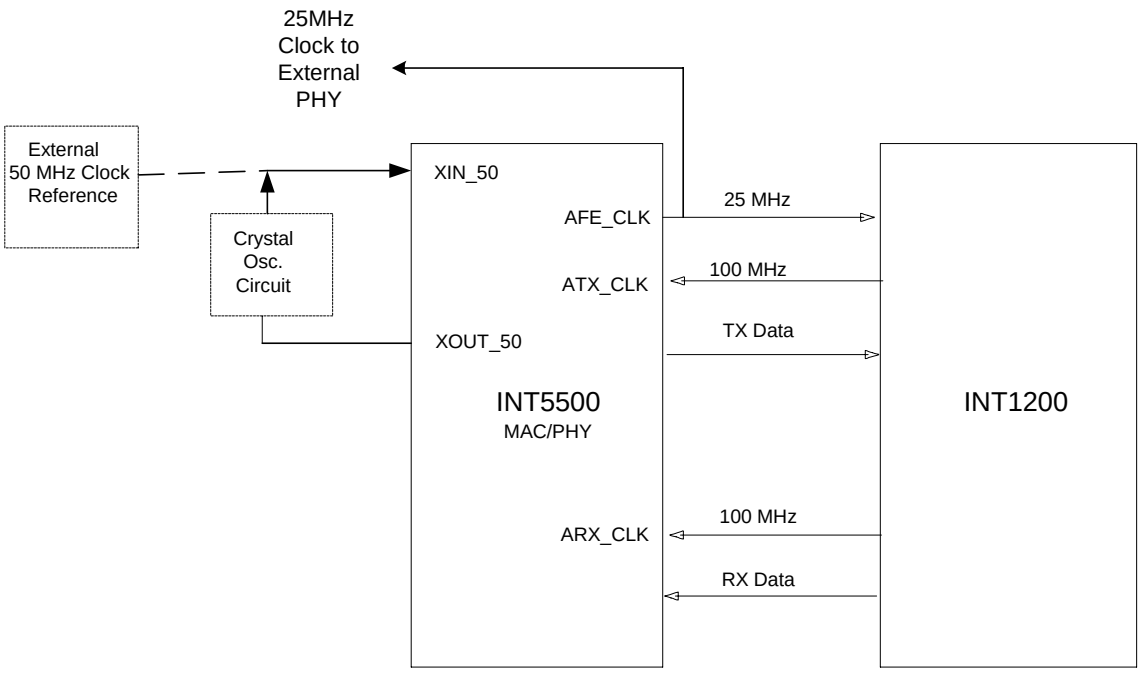


Figure 6: Recommended Clocking Arrangement for the INT5500 IC Based Designs

7.4. Crystal Oscillator Circuit

The recommended crystal circuit for the INT5500 based designs is shown in Figure 7 below. Intellon strongly recommends the use of a 3rd overtone 50 MHz crystal circuit to meet HomePlug clock accuracy requirements. The crystal must have a frequency tolerance of +/- 10 ppm in order to meet the HomePlug requirement of clock accuracy of 25 ppm over temperature, aging and manufacturing variations. Some recommended third overtone crystal parts are listed Table 5. Refer to Section 9.2 for crystal specifications.

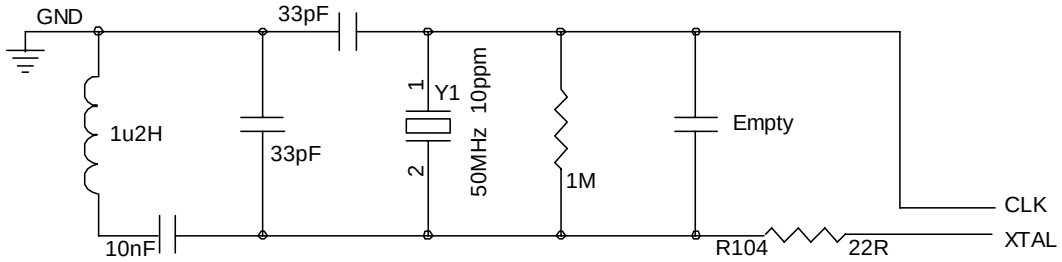


Figure 7: 3rd Overtone Crystal Circuit

Manufacturer	Part
ECS	ECS-500-18-5P-CK

Table 4: Recommended Crystal Part

Note: Care must be taken to ensure that the XIN_50 input does not exceed 3.3 V rail when it is driven from a clock oscillator or other remote source.

7.5. PLL Power Filtering

The INT5500 incorporates phase-locked loop (PLL) circuitry that multiplies the master 50 MHz reference clock in order to generate higher frequency clocks required for internal operation and for the attached INT1200 IC. The PLL power supply pins are brought out to dedicated pins (VAD and VAS) so that external filtering can be applied to minimize system noise coupling into the PLL. It is important to provide the cleanest possible power to the VAD pin in order to minimize the jitter produced in clocks generated by the PLL. The recommended filtering arrangement is illustrated in shown in Figure 8.

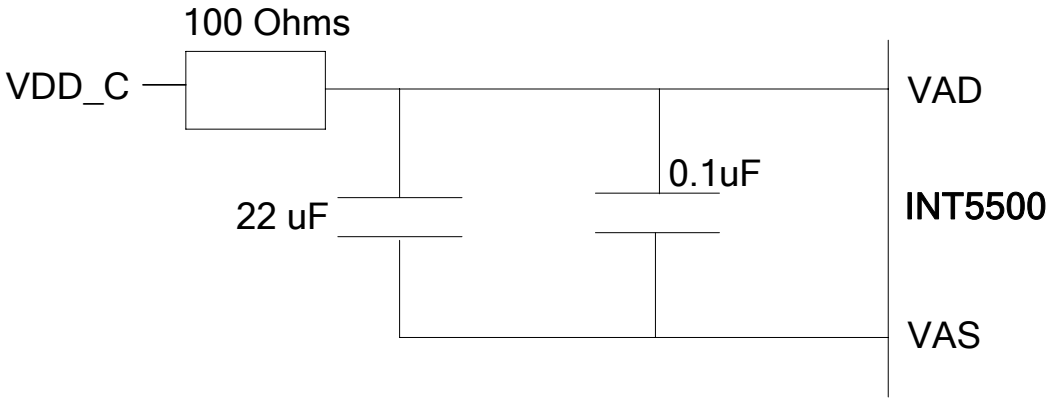


Figure 8: Recommended PLL Power Filtering

7.6. LED Function/GPIO Strapping

7.6.1. LED Functions

The function of LEDs connected to GPIO pins 1 through 4 is completely configurable. There are several LED indicator functions that can be selected and LED functions can be associated with GPIO pins on a pin-by-pin basis.

The following LED indicator functions can be selected through the Configuration Block (refer INT5500 SDK technical guide):

- Powerline Link/Activity
- Ethernet Link/Activity
- Collision
- Link status
- Network Status
- Turbo Status

The recommended LED mapping is shown below:

1. Powerline Link/Activity (GPIO1)—LED connected to GPIO1 indicates Powerline Link/Activity.
2. Ethernet Link/Activity (GPIO2)—LED connected to GPIO2 indicates Ethernet Link/Activity.
3. Turbo Status (GPIO3)—LED connected to GPIO3 indicates Turbo Status.
4. Power (GPIO4)—LED connected to GPIO4 indicates Power.

7.6.2. GPIO Strapping

GPIO Strapped High and low in Figure 9 and 10 respectively illustrate how a pull-up or pull-down configuration strap is combined with an LED

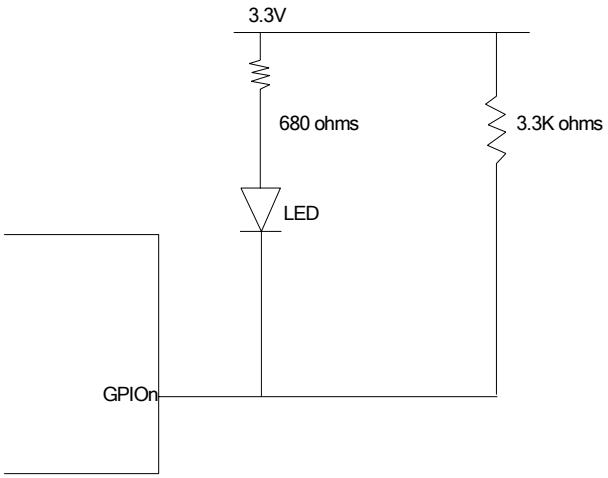


Figure 9: GPIO Strapped High

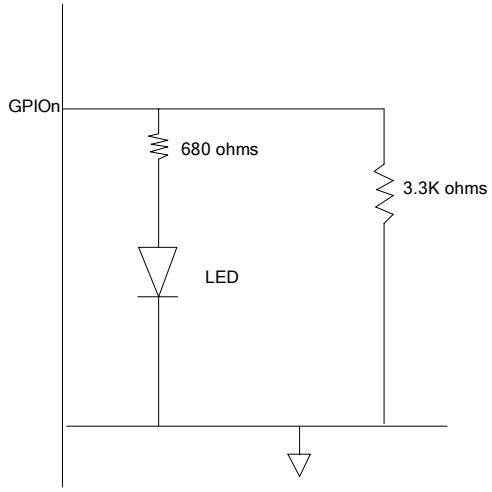


Figure 10: GPIO Strapped Low

7.7. 5-V Tolerance of Input

All inputs are 5-V tolerant except for XIN_50, ATX_CLK and ARX_CLK. The signal levels presented to these inputs must not exceed the I/O supply voltage (nominal 3.3 V). The ATX_CLK and ARX_CLK signals are driven directly from the INT1200 IC, which use either a 3.3 V or 2.5 V supply, so this requirement is easily met for these two inputs. Care must be taken to ensure that the XIN_50 input does not exceed 3.3 V rail when it is driven from a clock oscillator or other remote source.

8. User Protocol Interface

8.1. HomePlug MAC Management Entries

HomePlug MAC Management Entries (MME) may appear in any frame processed by the INT5500. The INT5500 utilizes the MAC Management Information format as specified in the HomePlug 1.0.1 Specification as a basis for MMEs. The basic format for the MME is shown below.

Unless otherwise noted all multi-byte fields have a big-endian byte order.

HomePlug MAC Management Entry Frame Format

	Field	Length	Definition
	DA	6 octets	IEEE formatted destination address
	SA	6 octets	IEEE formatted source address
HomePlug MAC Management Entries (MMEs)	MTYPE	2 octets	0x887B (IEEE assigned Ethertype for HomePlug devices) The presence of the MAC Management Information field is indicated when the first two bytes following the SA of a frame has the value 0x887B.
	MCTRL	1 octet	MAC Control Field The 8-bit MAC Control field indicates the number of MAC data entries contained in the MAC Management Information field.
	MEHDR	1 octet	First MAC Management Entry Header
	MELEN	1 octet	First MAC Management Entry Length [=N_1] The MAC Entry Length field contains the length in octets of the MMENTRY field. If MMENTRY does not exist, MELEN is set to zero. This field provides for transparent extension of MAC management, without rendering older equipment obsolete. If a frame is received with an METYPE value that is not understood, the receiver can still properly parse the frame and process its contents, ignoring what it does not understand.
	MMENTRY	N_1 octets	First MAC Management Entry Data
	• • •		
	MEHDR	1 octet	Last MAC Management Entry Header
	MELEN	1 octet	Last MAC Management Entry Length [=N_L]
	MMENTRY	N_L octets	Last MAC Management Entry
	Ethertype	2 octets	Optional Ethertype
	Data	N octets	Optional payload data

MAC Control Field (MCTRL)

Field	Bit Number	Bits	Definition
RSVD	7	1	Reserved.
NE	6-0	7	Number Of MAC Data Entries The 7-bit Number of MAC Entries field indicates the number of MAC data entries (defined as a MAC Entry Header and MAC Entry Data pair) following in the MAC Management Information Field.

MAC Entry Header Field (MEHDR)

Field	Bit Number	Bits	Definition
MEV	7-5	3	MAC Entry Version The 3-bit MAC Entry Version field indicates the version in use for interpretation of MAC Entries. Transmitter shall set to all zeros for this version, receiver shall decode and discard the entire MAC Management Information Field if MEV≠0b000.
METYPE	4-0	5	MAC Entry Type The 5-bit MAC Entry Type field defines the MAC entry command or request which follows. The combination of the METYPE and MDATA form a MAC entry.

The table below defines METYPE fields and the manner in which they are used by the MAC. The "M1 Interface" column indicates whether the METYPE appears on the M1 interface. The "Prepend to host MSDU" column indicates whether the METYPE is allowed to be inserted at the front of a host MSDU that is being processed for transmission by the MAC. "Only" in this column indicates that this METYPE is only used in conjunction with an MSDU.

NOTE: The M1 interface is defined as the "host" interface to the INT5500. In the INT5500 (PHY Option), the host is the entity on the other side of the MII PHY interface (typically an Ethernet controller or microprocessor). In the INT5500 (Host/DTE Option), the host is any entity on the other side of the MII Host/DTE interface (assuming the PHY is connected to an Ethernet sub network, the host is any device on the Ethernet sub network).

MAC Entry Type Field (METYPE)

METYPE Value [4…0]	Interpretation	M1 Interface	Prepend to host MSDU
0 0000	Request Channel Estimation	No	Allowed
0 0001	Channel Estimation Response	No	Allowed
0 0010	Vendor Specific	Yes	Allowed
	Get Device Description Request	Only	No
	Get Device Description Response	Only	No
	Get Channel Capacities Request	Only	No
	Get Receive Channel Capacities Response	Only	No
	Get Transmit Channel Capacities Response	Only	No
0 0011	Replace Bridge Address	No	Only
0 0100	Set Network Encryption Key	Yes	Allowed
0 0101	Multicast With Response	No	Only
0 0110	Confirm Network Encryption Key	Yes	Allowed
0 0111	Request Parameters and Statistics	Yes	Allowed
0 1000	Parameters and Statistics Response	Yes	Allowed
0 1001-0 1111	Reserved METYPE on transmit, skip entire layer management entry on receive	No	Allowed
1 0000-1 1000	Manufacturer-specific METYPE space. Never transmitted on medium.	Only	No
1 0010	Intellon Specific MME	Only	No
	Get Device Version Request	Only	No
	Get Firmware Version Request	Only	No
	Get Local Bridge Proxy Addresses Request	Only	No
	Get Remote Bridge Proxy Addresses Request	Only	No

METYPE Value [4…0]	Interpretation	M1 Interface	Prepend to host MSDU
1 0011	Get Device Version Request Response	Only	No
	Get Firmware Version Request Response	Only	No
	Get Local Bridge Proxy Addresses Request Response	Only	No
	Get Remote Bridge Proxy Addresses Request Response	Only	No
1 0100	Encryption Key Tag	Only	No

8.1.1. MAC Management Entries (MMEs)

8.1.1.1. Request Channel Estimation (METYPE – 0x00)

Request Channel Estimation is a one-byte MME indicating the channel estimation version capability of the requestor, which causes the receiving station to return Channel Estimation.

This MME is described for information only. This MME will not appear on the host M1 interface.

Request Channel Estimation (METYPE – 0x00)

Field	Byte	Bit Number	Bits	Definition
CEV	0	7-4	4	Channel Estimation Version The 4-bit Channel Estimation Version field indicates the channel estimation version level capability of the station transmitting the request. CEV is set to all zeros for the INT5500.
RSVD		3-0	4	Reserved on transmit, ignore on receive

8.1.1.2. Channel Estimation Response (METYPE – 0x01)

Channel Estimation Response is a variable length MME sent by a device after receiving a Channel Estimation Request MME. This sequence is part of the channel estimation control.

This MME is described for information only. This MME will not appear on the host M1 interface.

Channel Estimation Response (METYPE – 0x01)

Field	Byte	Bit Number	Bits	Definition
CERV	0	7-4	4	Channel Estimation Response Version The 4-bit Channel Estimation Response Version field indicates the response version in use. CERV is set to all zeros for the INT5500.
RSVD		3-0	4	Reserved on transmit, ignored on receive
	1	7-5	3	
RXTMI		4-0	5	Receive Tone Map Index The 5-bit Receive Tone Map Index field contains the value to be associated with the Source Address of the station returning the Channel Estimation Response. The station receiving this response inserts the Receive Tone Map Index value in the TMI field of the Start of Frame delimiter when transmitting to the responder.
VT [79-0]	2	7-0	8	Valid Tone Flags [7-0] Valid Tone Flags indicate whether a specific tone is valid (VT[x]=0b1) or invalid (VT[x]=0b0).
	3	7-0	8	Valid Tone Flags [15-8]
	4	7-0	8	Valid Tone Flags [23-16]
	5	7-0	8	Valid Tone Flags [31-24]
	6	7-0	8	Valid Tone Flags [39-32]
	7	7-0	8	Valid Tone Flags [47-40]
	8	7-0	8	Valid Tone Flags [55-48]
	9	7-0	8	Valid Tone Flags [63-56]
	10	7-0	8	Valid Tone Flags [71-64]
	11	7-0	8	Valid Tone Flags [79-72]

Field	Byte	Bit Number	Bits	Definition
RATE	12	7	1	FEC Rate The FEC Rate bit indicates whether the convolutional coding rate is ½ (RATE=0b0) or ¾ (RATE=0b1).
BP		6	1	Bridge Proxy Bridge Proxy indicates that the tone map is being proxied for the following DAs. NBDAS and BDAn only exist if BP=0b1.
MOD		5-4	2	Modulation Method 00: ROBO Modulation 01: DBPSK Modulation 10: DQPSK Modulation 11: Reserved on transmit, ignore on reception
VT[83-80]		3-0	4	Valid Tone Flags [83-80]
RSVD	13	7	1	Reserved on transmit, ignore on receive
NBDAS		6-0	7	Number Bridged Destination Addresses The Number Bridged Destination Addresses and Bridged Destination Addresses only exist if BP=0b1. NBDAS indicate the number of proxied DA, and BDAn contains the addresses. Up to 16 BDAs are included in the Channel Estimation Response for the INT5500. NOTE: The INT5500 (Host/DTE Option) will store up to 64 BDAs for use in its address filtering function.
BDA1	14-19	--	48	Bridged Destination Address #1
• • •				

8.1.1.3. Vendor Specific Parameters (METYPE – 0x02)

Vendor Specific field is a variable length MME that allows vendor specific extensions to the HomePlug 1.0.1 Specification. The first 3 bytes of the entry should be an IEEE assigned Organizationally Unique Identifier (OUI).

Vendor Specific Parameters Field (METYPE – 0x02)

Field	Byte	Bit Number	Bits	Definition
OUI	0	7-0	8	OUI [23-16] 0x00
	1	7-0	8	OUI [15-8] 0x04
	2	7-0	8	OUI [7-0] 0x87
Vendor Defined	3-255	--	--	Vendor Defined

Note: Intellon private MMEs are described in section 8.1.2.

8.1.1.4. Replace Bridge Address (METYPE – 0x03)

The Replace Bridge Address MME contains a 6-byte MAC Original Destination Address of a device, which may be on another medium and accessed via a bridge and a 6-byte MAC Original Source Address of a device, which may be on another medium and accessed via a bridge. The station receiving this MAC Entry reconstructs the original MSDU using the ODA and OSA contained in this entry. The ODA and OSA Fields (6 bytes each) are in IEEE 48-bit MAC address format.

This MME is described for information only and will not appear on the host M1 interface.

Replace Bridge Address Field (METYPE – 0x03)

Field	Byte	Bit Number	Bits	Definition
ODA[47-0]	0	7-0	8	Original Destination Address, first octet
	1	7-0	8	Original Destination Address, second octet
	2	7-0	8	Original Destination Address, third octet
	3	7-0	8	Original Destination Address, fourth octet
	4	7-0	8	Original Destination Address, fifth octet
	5	7-0	8	Original Destination Address, sixth octet
OSA[47-0]	6	7-0	8	Original Source Address, first octet
	7	7-0	8	Original Source Address, second octet
	8	7-0	8	Original Source Address, third octet
	9	7-0	8	Original Source Address, fourth octet
	10	7-0	8	Original Source Address, fifth octet
	11	7-0	8	Original Source Address, sixth octet

8.1.1.5. Set Network Encryption Key (METYPE – 0x04)

The HomePlug Set NEK MME is used to perform Network Encryption Key changes.

When this MME is received (a unicast destination address matching the station address or the broadcast destination address) is processed by the INT5500 according to the following rules.

If the INT5500 is operating in Host/DTE or PHY mode:

- If a unicast HomePlug Set NEK MME is received from the host and it is addressed to the Local Station Address or the Local Management Address, the INT5500 will accept the key change, update its Non-volatile Parameters (in NVRAM), and return a HomePlug Confirm NEK MME to the host.
- If a unicast HomePlug Set NEK MME is received from the host and it is not addressed to the Local Station Address or the Local Management Address (i.e. it's destined for a remote station) it will be forwarded to the power line.
- If a broadcast Set NEK MME is received from the host the INT5500 will forward the Set NEK MME to the power line.
- If a unicast or broadcast Set NEK MME is received from the power line that was encrypted with the station's Default Encryption Key the INT5500 will accept the key change, update its Non-volatile Parameters (in NVRAM), and return a HomePlug Confirm NEK MME to the originating address.
- If a unicast or broadcast Set NEK MME is received from the power line that wasn't encrypted with the station's Default Encryption Key the INT5500 will discard the request.

Note 1: The process of updating the Non-volatile Parameters can take between 100 milliseconds and 4 seconds; this is due to the length of time required to erase a Serial Flash sector.

Note 2: During the time while the MAC is updating its non-volatile parameters the new key will be active. If another Set NEK MME is sent to the MAC before it returns the Confirm NEK MME the second Set NEK MME will be ignored and no confirm will be sent.

Note 3: If the Confirm NEK MME is not received in response to a Set NEK MME the application that initiated the key change should NOT make any assumptions about which key the station is using; it may be still using the old key (i.e. the Set NEK MME was lost or ignored), it may be using the new key (i.e. the Confirm NEK MME was lost), or it may be using an entirely different key (i.e. another key change was already in progress). Ultimately the device can be recovered from this state by repeating the Set NEK operation.

Note 4: It is STRONGLY RECOMMENDED that all remote Set NEK MMEs are sent to the Broadcast Address to insure that the MME is sent in ROBO mode on the powerline. Since remote Set NEK MMEs are encrypted with a unique DEK so that only one device will respond with a Confirm NEK MME.

If the INT5500 is operating in Host Boot Mode (INT5500 is initialized via the host interface):

- If a unicast HomePlug Set NEK MME is received from the host and it is addressed to the Local Station Address or the Local Management Address, the INT5500 will accept the key change, and return a HomePlug Confirm NEK MME to the host.
- If a unicast HomePlug Set NEK MME is received from the host and it is not addressed to the Local Station Address or the Local Management Address (i.e. it's destined for a remote station) it will also be forwarded to the power line.
- If a broadcast Set NEK MME is received from the host the INT5500 will forward the Set NEK MME to the power line.
- If a unicast or broadcast Set NEK MME is received from the power line that was encrypted with the station's Default Encryption Key the INT5500 will forward the Set NEK MME to the host.
- If a unicast or broadcast Set NEK MME is received from the power line that wasn't encrypted with the station's Default Encryption Key the INT5500 will discard the request.

In Host Boot Mode it is the responsibility of the Host to maintain the Non-volatile Parameters.

Note: If a Set NEK MME is sent to the INT5500 with the NewEKS field set to 0, the Default Encryption Key will be replaced. If the Default Encryption Key is changed, there is no easy method to revert to the original (or previous) Default Encryption Key.

Set Network Encryption Key Field (METYPE – 0x04)

Field	Byte	Bit Number	Bits	Definition
EKS	0	7-0	8	Encryption Key Select The one-byte EKS field is associated with the Network Encryption Key. Encrypted data transport uses the EKS value to indicate which NEK is to be used for decryption.
NEK	1	7-0	8	Network Encryption Key, first octet The 64-bit Network Encryption Key field contains the key that is to be stored locally in non-volatile storage and is to be used for subsequent encryption under control of EKS.
	2	7-0	8	Network Encryption Key, second octet
	3	7-0	8	Network Encryption Key, third octet
	4	7-0	8	Network Encryption Key, fourth octet
	5	7-0	8	Network Encryption Key, fifth octet
	6	7-0	8	Network Encryption Key, sixth octet
	7	7-0	8	Network Encryption Key, seventh octet
	8	7-0	8	Network Encryption Key, eight octet

The network encryption key is saved and usable after receipt of the Set Network Encryption Key MME. If a device using an INT5500 contains a serial flash; the network encryption key is also automatically stored in a nonvolatile manner and reloaded after power cycling.

8.1.1.6. Multicast with Response (METYPE – 0x05)

When given a Host frame with a multicast address, the INT5500 will prepend the Multicast With Response MME to allow it to direct the Powerline frame to a device, which will act as the response proxy for the frame. Multicast With Response is a 6-byte MME containing the actual multicast destination address. The DA contained in the layer management MAC frame is the unicast proxy for the multicast and will generate an ACK/NACK/FAIL response if requested. The proxy will be selected in a round-robin fashion from devices in the INT5500's network information table (nodes from which channel estimation responses have been received).

When given a Host frame with a unicast address that is unknown, the INT5500 will use the Replace Bridge Address MME and replace the DA of the frame with the Universal Broadcast address. This is done to facilitate the case where the unknown ODA is accessed through a bridge. This altered frame will be treated the same as a Host addressed frame destined to a multicast address and Multicast With Response will be prepended.

Note: Multicast Frames with or without a proxy will be transmitted using ROBO modulation, because ROBO is the only tone map that can be universally demodulated.

This MME is described for information only and will not appear on the host M1 interface.

8.1.1.7. Confirm Network Encryption Key (METYPE – 0x06)

The Confirm Network Encryption Key MME is transmitted in response to the proper reception and execution of a Set Network Encryption Key MME. This entry shall be encrypted with the Network Encryption Key received in the Set Network Encryption Key command causing the response.

This is a zero-byte (null) entry and is indicated by the METYPE only. MELEN is set to zero.

- When operating in Host/ DTE or PHY Modes the INT5500 generates the Confirm NEK MME.
- When operating in Host Boot Mode, the host is required to generate the Confirm NEK MME.
- In both cases, Confirm NEK MMEs will be forwarded from the power line to the host.

8.1.1.8. Request Parameters and Statistics (METYPE – 0x07)

The HomePlug Request Parameters and Statistics MME is a zero-byte (null) entry sent to retrieve common HomePlug statistics from stations. This MME is also used as part of Station Discovery.

When this MME is received from the host, the INT5500 will return a HomePlug Parameters and Statistics Response MME. If the request was sent to the Broadcast Address, it will also be forwarded to the powerline.

When this MME is received from the powerline, the INT5500 will return a HomePlug Parameters and Statistics Response MME. This MME will not be forwarded from the powerline to the host.

8.1.1.9. Parameters and Statistics Response (METYPE – 0x08)

The HomePlug Parameters and Statistics Response MME is sent by the INT5500 in response to a HomePlug Request Parameters and Statistics MME.

Note: All of the statistics counters in the table below are reset at power up.

Parameters and Statistics Response Field (METYPE – 0x08)

Field	Byte	Bit Number	Bits	Definition
TXACK[15-0]	0	7-0	8	Transmit ACK Counter [15-8] The 16-bit Transmit ACK Counter increments when an ACK is received after transmitting a PHY Frame with response expected.
	1	7-0	8	Transmit ACK Counter [7-0]
TXNACK[15-0]	2	7-0	8	Transmit NACK Counter [15-8] The 16-bit Transmit NACK Counter increments when a NACK is received after transmitting a PHY Frame with response expected.
	3	7-0	8	Transmit NACK Counter [7-0]
TXFAIL[15-0]	4	7-0	8	Transmit FAIL Counter [15-8] The 16-bit Transmit FAIL Counter increments when a FAIL is received after transmitting a PHY Frame with response expected.
	5	7-0	8	Transmit FAIL Counter [7-0]
TXCLOSS[15-0]	6	7-0	8	Transmit Contention Loss Counter [15-8] The 16-bit Transmit Contention Loss Counter increments when the station defers to another transmitting station with the same transmit priority during the Contention Window.
	7	7-0	8	Transmit Contention Loss Counter [7-0]
TXCOLL[15-0]	8	7-0	8	Transmit Collision Counter [15-8] The 16-bit Transmit Collision Counter increments when a Collision is inferred to have occurred, after transmitting a PHY frame for which a response is expected.
	9	7-0	8	Transmit Collision Counter [7-0]
TXCA3LAT[15-0]	10	7-0	8	Transmit CA3 Latency Counter [15-8] The 16-bit Transmit CA3 Latency Counter contains the cumulative total of number of milliseconds from receipt of a CA3 priority transmit request to successful transmit completion or transmit timeout. Subsequent Collisions do not affect this metric.
	11	7-0	8	Transmit CA3 Latency Counter [7-0]
TXCA2LAT[15-0]	12	7-0	8	Transmit CA2 Latency Counter [15-8] The 16-bit Transmit CA2 Latency Counter contains the cumulative total of number of milliseconds from receipt of a CA2 priority transmit request to successful transmit completion or transmit timeout. Subsequent Collisions do not affect this metric.
	13	7-0	8	Transmit CA2 Latency Counter [7-0]
TXCA1LAT[15-0]	14	7-0	8	Transmit CA1 Latency Counter [15-8] The 16-bit Transmit CA1 Latency Counter contains the cumulative total of number of milliseconds from receipt of a CA1 priority transmit request to successful transmit completion or transmit timeout. Subsequent Collisions do not affect this metric.
	15	7-0	8	Transmit CA1 Latency Counter [7-0]

Field	Byte	Bit Number	Bits	Definition
TXCA0LAT[15-0]	16	7-0	8	Transmit CA0 Latency Counter [15-8] The 16-bit Transmit CA0 Latency Counter contains the cumulative total of number of milliseconds from receipt of a CA0priority transmit request to successful transmit completion or transmit timeout. Subsequent Collisions do not affect this metric.
	17	7-0	8	Transmit CA0 Latency Counter [7-0]
RXBP40[31-0]	18	7-0	8	Receive Cumulative Bytes per 40-symbol Packet Counter [31-24] The 32-bit Receive Cumulative Bytes per 40-symbol Packet Counter contains the cumulative total of number of bytes within a received 40-symbol packet for each validly received PHY frame. The number of bytes is based on the tone map and modulation characteristics.
	19	7-0	8	Receive Cumulative Bytes per 40-symbol Packet Counter [23-16]
	20	7-0	8	Receive Cumulative Bytes per 40-symbol Packet Counter [15-8]
	21	7-0	8	Receive Cumulative Bytes per 40-symbol Packet Counter [7-0]

8.1.2. INT5500 Private MMEs

INT5500 Private MMEs are HomePlug Manufacturer Specific MMEs that are used to query and control the INT5500 MAC.

The MMEs listed in this section are targeted primarily towards INT5500 with Boot from Serial Flash (standalone mode). Customers using the INT5500 PHY Option for Embedded Applications (Boot from Host) shall refer to the **INT5500 Software Development Kit** (contains complete list of MMEs and function calls).

Unless otherwise noted, all MMEs listed below must contain one and only one MME per Ethernet Frame.

8.1.2.1. Get Device Description MME

METYPE: 0x02
MID: 16
DA: *Broadcast* or *StationAddress*

The Get Device Description Data MME retrieves the Manufacturer Name and Product Name of an INT5500 based station; this MME also returns the MAC Version and an indication of whether the INT5500 is local (i.e. communicating with the requestor via the host interface) or remote (i.e. communicating with the requestor via the powerline).

Get Device Description Request MME

Field	Byte	Bit Number	Bits	Definition	Value
OUI	0	7-0	8	OUI [23-16]	0x00
	1	7-0	8	OUI [15-8]	0x04
	2	7-0	8	OUI [7-0]	0x87
MMEDirection	3	7	1	Direction of MME Request [or] Response	**0** [Request]
MID		6-0	7	Message ID	**16**

Get Device Description Response MME

Field	Byte	Bit Number	Bits	Definition	Value
OUI	0	7-0	8	OUI [23-16]	0x00
	1	7-0	8	OUI [15-8]	0x04
	2	7-0	8	OUI [7-0]	0x87
MMEDirection	3	7	1	Direction of the MME. Request [or] Response	**1** [Response] Mask off this bit to get MID
MID		6-0	7	Message ID	**16**
Reserved	4	7-2	6	Reserved	0
ProtocolVersionFlag		1	1	Protocol Version	1—Refer table below
ConnectionFlag		0	1	Local or Remote Connection Flag	0—If the station is local 1—If the station is remote
ProtocolVersion	5-8	--	32	MAC FW Protocol Version	See below
ManufacturerStringLen	9	--	8	Length of Manufacturer's String	
ManufacturerString []	Variable	--	--	Manufacturer String	Manufacturer string, not NULL terminated
ProductNameStringLen	--	--	8	Length of the Product Name String	
ProductNameString []	Variable	--	--	Product Name String	Product name string, not NULL terminated

ProtocolVersion

*If the **ProtocolVersionFlag** field is set to 0, the **ProtocolVersion** field will contain the value 0x11011001 for MAC version 1.2.*

*If the **ProtocolVersionFlag** field is set to 1, the **ProtocolVersion** field will contain a protocol version encoded as shown below.*

Protocol Version Field

Field	Byte	Bit Number	Bits	Definition	Value
ProtocolIdentifier	2 bytes	--	16	Protocol Identifier	0x5500
ProtocolVersionMajor	1 byte	7-4	4	Protocol Version Major	**1** (for MAC **1**.5)
ProtocolVersionMinor		3-0	4	Protocol Version Minor	**5** (for MAC 1.**5**)
ProtocolReserved	1 byte	--	8	Protocol Reserved	Reserved

8.1.2.2. Get Channel Capacities MME

METYPE: 0x02
MID: 24
MELEN: Channel Capacities Request MME—5
Channel Capacities Response MME—Variable
DA: Broadcast or *StationAddress*

The Get Channel Capacities Request MME retrieves receive or transmit channel capacities of INT5500 based station.

Get Channel Capacities Request MME

Field	Byte	Bit Number	Bits	Definition	Value
OUI	0	7-0	8	OUI [23-16]	0x00
	1	7-0	8	OUI [15-8]	0x04
	2	7-0	8	OUI [7-0]	0x87
MMEDirection	3	7	1	Direction of MME Request [or] Response	**0** [Request]
MID		6-0	7	Message ID	**24**
DirectionFlag	4	--	8	Receive/Transmit Capacities	0—Request Receive Capacities 1—Request Transmit Capacities

The Direction Flag field is set to "0" or "1" depending on the receive response or the transmit response.

Get Receive Channel Capacities Response MME (Request DirectionFlag = 0)

Field	Byte	Bit Number	Bits	Definition	Value
OUI	0	7-0	8	OUI [23-16]	0x00
	1	7-0	8	OUI [15-8]	0x04
	2	7-0	8	OUI [7-0]	0x87
MMEDirection	3	7	1	Direction of MME Request [or] Response	**1** [Response]
MID		6-0	7	Message ID	**24**
Message Data					
RX_Station 1					
RemoteStationAddress[6]	6 bytes	--	48	Remote Station MAC Address	--
RxBytesPerBlock	2 bytes	--	16	Bytes per 336 µs block	--
Reserved[6]	6 bytes	--	48	Reserved	--
RX_Station 2					
RemoteStationAddress[6]	6 bytes	--	48	Remote Station MAC Address	--
RxBytesPerBlock	2 bytes	--	16	Bytes per 336 µs block	--
Reserved[6]	6 bytes	--	48	Reserved	--
• • •					
RX_Station N					
RemoteStationAddress[6]	6 bytes	--	48	Remote Station MAC Address	--
RxBytesPerBlock	2 bytes	--	16	Bytes per 336 µs block	--
Reserved[6]	6 bytes	--	48	Reserved	--

The value of MELEN for Receive Response MME is variable.
*MELEN = [14 bytes/remote station * N_RX_STATIONS (maximum 16 stations)]*

Get Transmit Channel Capacities Response MME (Request DirectionFlag = 1)

Field	Byte	Bit Number	Bits	Definition	Value
OUI	0	7-0	8	OUI [23-16]	0x00
	1	7-0	8	OUI [15-8]	0x04
	2	7-0	8	OUI [7-0]	0x87
MME Direction	3	7	1	Direction of MME Request [or] Response	**1** [Response]
MID		6-0	7	Message ID	**24**
Message Data					
TX_Station 1					
RemoteStationAddress[6]	6 bytes	--	48	Remote Station MAC Address	--
TxBytesPerBlock	2 bytes	--	16	Transmit Bytes per 336 µs block	--
TX_Station 2					
RemoteStationAddress[6]	6 bytes	--	48	Remote Station MAC Address	--
TxBytesPerBlock	2 bytes	--	16	Transmit Bytes per 336 µs block	--
• • •					
TX_Station N					
RemoteStationAddress[6]	6 bytes	--	48	Remote Station MAC Address	--
RxBytesPerBlock	2 bytes	--	16	Bytes per 336 µs block	--

The value of MELEN is for the Transmit Response MME is variable.
*MELEN = [8 bytes/remote station * N_TX_Stations (maximum 32 stations)]*

8.1.2.3. Get Device Version MME

METYPE: 0x12
MID: 1
MMELEN: 1
DA: *StationAddress*

The Get Device Version MME returns the device version of the INT5500.

Get Device Version Request

Field	Byte	Bit Number	Bits	Definition	Value
MID	1 byte	7-0	8	Message ID	**1**

8.1.2.4. Get Device Version Response MME

METYPE: 0x13
MID: 1
MMELEN: 1
DA: *StationAddress*

Get Device Version Response MME

Field	Byte	Bit Number	Bits	Definition	Value
MID	1 byte	7-0	8	Message ID	**1**
DeviceVersion String	Variable				**INT5500CS**

8.1.2.5. Get Firmware Version MME

METYPE: 0x12
MID: 32
MMELEN: 1
DA: *StationAddress*

The Get Firmware Version MME returns the INT5500 MAC firmware version string.

Get Firmware Version Request

Field	Byte	Bit Number	Bits	Definition	Value
MID	1 byte	7-0	8	Message ID	**32**

8.1.2.6. Get Firmware Version Response MME

METYPE: 0x13
MID: 32
MMELEN: 1
DA: *StationAddress*

Get Firmware Version Response

Field	Byte	Bit Number	Bits	Definition	Value
MID	1 byte	7-0	8	Message ID	**32**
FirmwareVersion String	Variable				**See next page**

FirmwareVersionString

This contains the full version of the MAC firmware. The typical format of this string is:

"INT5500CS MAC-*firmware.Version-firmware.BuildDate-firmware.BuildType*"

where,

firmware.Version is of the format

"Major-Minor-Increment-Build"

The version number for MAC 1.4 is **"1-4-3-19"**
The version number for MAC 1.5 is **"1-5-5-53"**

firmware.BuildDate is of the format

"yyyymmdd"

The build date for MAC 1.4 is "**20050506"**
The build date for MAC 1.5 is "**20050712"**

firmware.BuildType indicates the type of build

8.1.2.7. Get Local Bridge Proxy Addresses

METYPE: 0x12
MID: 39
MMELEN: 1
DA: *StationAddress*

The Get Local Bridge Proxy Addresses MME returns a list of 48-bit IEEE MAC Addresses that are currently in the INT5500's Local Bridge Proxy Table. Up to 16 addresses are maintained in the Local Bridge Proxy table (and hence the maximum number of addresses returned by this MME is 16).

Get Local Bridge Proxy Address Request MME

Field	Byte	Bit Number	Bits	Definition	Value
MID	1 byte	7-0	8	Message ID	**39**

8.1.2.8. Get Local Bridge Proxy Addresses

METYPE: 0x13
MID: 39
MMELEN: Variable
DA: *StationAddress*

Get Local Bridge Proxy Address Response MME

Field	Byte	Bit Number	Bits	Definition	Value
MID	1 byte	7-0	8	Message ID	**39**
Address	6 bytes			MAC address of the first station	
			…		
Address	6 bytes			MAC address of the last station	

8.1.2.9. Get Remote Bridge Table

METYPE: 0x12
MID: 66
MMELEN: 1
DA: *StationAddress*

The Get Remote Bridge Table MME returns the mapping of 48-bit IEEE MAC Addresses to Remote Station Addresses (also 48-bit MAC addresses) that are currently in the INT5500's Remote Bridge Table. Up to 64 addresses are maintained in the Local Bridge Proxy table (and hence the maximum number of addresses returned by this MME is 64).

The Get Remote Bridge Table Response MME may contain more then one MME as the Remote Bridge Table can be more then 255 bytes in size. No assumptions should be made regarding the number of MMEs in the response or the number of entries per MME.

Get Remote Bridge Proxy Address Request MME

Field	Byte	Bit Number	Bits	Definition	Value
MID	1 byte	7-0	8	Message ID	**66**

8.1.2.10. Get Remote Bridge Table

METYPE: 0x13
MID: 66
MMELEN: Variable
DA: *StationAddress*

Get Remote Bridge Proxy Address Response MME

Field	Byte	Bit Number	Bits	Definition	Value
MID	1 byte	7-0	8	Message ID	**39**
Address	6 bytes			MAC address of the first station	
			…		
Address	6 bytes			MAC address of the last station	

8.1.2.11. Encryption Key Tag MME

METYPE: 0x14
MID: 1
DA: Any

The Encryption Key Tag MME instructs the INT5500 to send an MSDU with the specified Encryption Key Select and Encryption Key (by default the INT5500 will encrypt all outgoing powerline transmissions using current Network Encryption Key).

This MME is commonly used in Network Encryption Key setting operations. The following is the process flow for setting the Network Encryption Key:

- Host sends an MSDU to the INT5500. The Destination Address is set to the desired destination of the appended MSDU. Following the DA and SA fields, an Encryption Key Tag MME is inserted (along with the required MME prefix).
- The INT5500 detects the presence of the Encryption Tag MME and removes it. A side effect of this process is that the INT5500 bypasses packet aggregation. The actually MSDU is constructed by the INT5500 by concatenating the DA, SA and the Appending MSDU.
- The INT5500 encrypts the MSDU formed in step 2 with the alternate EK and alternate EKS specified in the Encryption Key Tag MME. This MSDU is sent to its final destination over the powerline.

The INT5500 cannot process an MSDU that contains more then 1518 bytes (including Source Address, Destination Address and Ethernet Type); as a result, it is not possible to send a full 1500 bytes of MSDU data when using an Encryption Key Tag MME.

The format of this MME is shown below.

Encryption Key Tag MME

Field	Byte	Bit Number	Bits	Definition	Value
TagMID	1 byte	7-0	8	Encryption Key Tag Message ID	**1**
EKS	1 byte	7-0	8	Encryption Key Select	EKS Value
EK7	1 byte	7-0	8	Encryption Key [63-56]	Encryption Key
EK6	1 byte	7-0	8	Encryption Key [55-48]	
EK5	1 byte	7-0	8	Encryption Key [47-40]	
EK4	1 byte	7-0	8	Encryption Key [39-32]	
EK3	1 byte	7-0	8	Encryption Key [31-24]	
EK2	1 byte	7-0	8	Encryption Key [23-16]	
EK1	1 byte	7-0	8	Encryption Key [15-8]	
EK0	1 byte	7-0	8	Encryption Key [7-0]	

9. Specifications

9.1. Electrical Specifications

9.1.1. Absolute Maximum Ratings for INT5500 IC

Operation at or above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to these conditions for extended periods of time may affect long-term device reliability. Correct functional behavior is not implied or guaranteed when operating at or above the Absolute Maximum Ratings.

Symbol	Parameter	Min	Max	Units
VDD_IO	I/O Supply Voltage (VDD_IO)	-0.3	3.6	V
VDD_C	Core Supply Voltage (VDD_CORE, VAD)	-0.3	1.98	V
VIN	Input Pin Voltage (CLK, ATX_CLK, ARX_CLK)	-0.5	3.9	V
	Input Pin Voltage (all pins excepts CLK, ATX_CLK, ARX_CLK)	-0.5	5.5	V
T_{STORE}	Storage Temperature	-40	125	^{O}C
V_{ESD}	Electrostatic Discharge		1000	V

Recommended Operating Conditions for INT5500 IC

Symbol	Parameter	Min	Typ	Max	Units
VDD_IO	I/O Supply Voltage (VDD_IO)	3.0	3.3	3.6	V
VDD_C	Core Supply Voltage (VDD_CORE, VAD)	1.62	1.8	1.98	V
T_A	Ambient Operating Temperature	0		70	^{O}C

DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
V_{OL}	Low-level output voltage	I_{OL}= 4, 6, 12 mA[1]			0.4	V
V_{OH}	High-level output voltage	I_{OH}=-4, -6, -12mA[2]	2.4			V
I_{IL}	Low-level input current	V_I = Gnd	-1			µA
I_{IH}	High-level input current	V_I = Vdd			1	µA
I_{OZ}	High-impedance output current	Gnd ≤ V_I ≥ Vdd	-1		+1	µA
I_{DD_CORE}	Dynamic current (VDD_C)			325		mA
I_{DD_IO}	Dynamic current (VDD_IO)			30		mA
C_{IN}	Pin capacitance	F_C = 1 MHz			5	pF

1. **I_{OL} = 4 mA for SPI_CLK, SPI_CS and SPI_DO.**
   I_{OL} = 12 mA for ASC_DATA, ASC_CLK, ASC_EN, AFE_PWRDN and GPIO [6:1].
   I_{OL} = 6 mA for all other output or bidirectional pins.

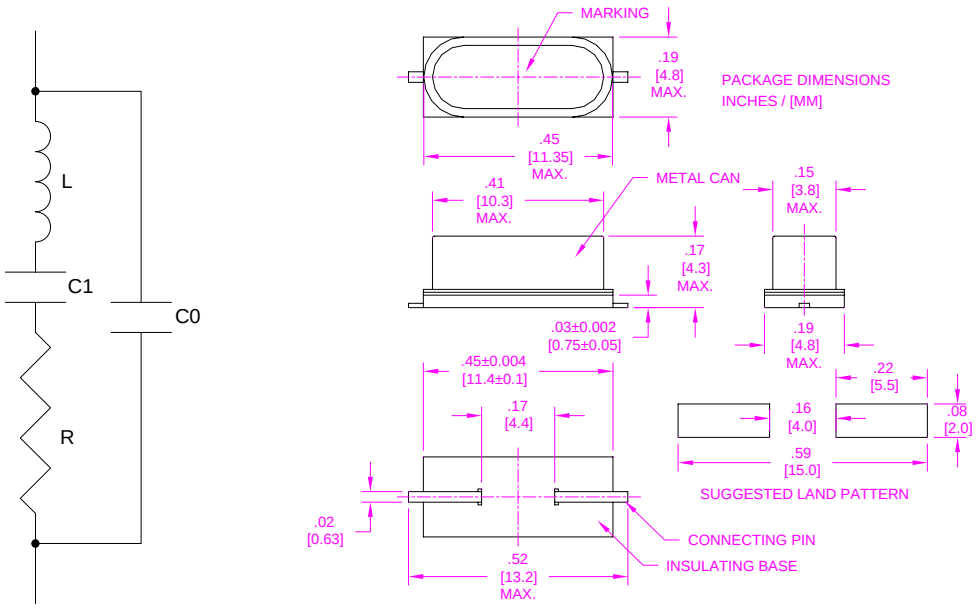
2. **I_{OH} = -4 mA for SPI_CLK, SPI_CS and SPI_DO.**
   I_{OH} = -12 mA for ASC_DATA, ASC_CLK, ASC_EN, AFE_PWRDN and GPIO [6:1].
   I_{OH} = -6 mA for all other output or bidirectional pins.

9.2. Crystal Specifications

Crystal Specifications

Parameters	Value
Mode:	3rd Overtone
Type:	AT strip resonator
Frequency:	50.000 MHz
Frequency Tolerance:	±10 ppm (Max) @ 25°C
Temperature Range:	-10°C to +70°C
Frequency Stability over Temperature:	±15 ppm (Max)
Aging:	±2 ppm/year
Load Capacitance:	18 pF
Package:	CSM-7 (4.3 mm)
Power Dissipation:	100 µW
C0:	4.1 pF (Typ) 7 pF (Max)
R(ESR):	80 Ω (Max)
C1:	Not specified
L:	Not specified
Q:	Not specified

SUGGESTED MANUFACTURER	
MANUFACTURER	**PART NUMBER**
ECS INC. INTERNATIONAL 1105 S. RIDGEVIEW OLATHE, KS 66062 U.S.A. (913) 782-7787	ECS-500-18-5P-CK-TR



9.3. Thermal Specification

Following table lists out the thermal parameters for the INT5500 IC.

Parameter	Value
θ_{JA}	32.0°C/W (with 0 m/s air flow)
θ_{JC}	6.6°C/W
Ψ_{JT}	0.4

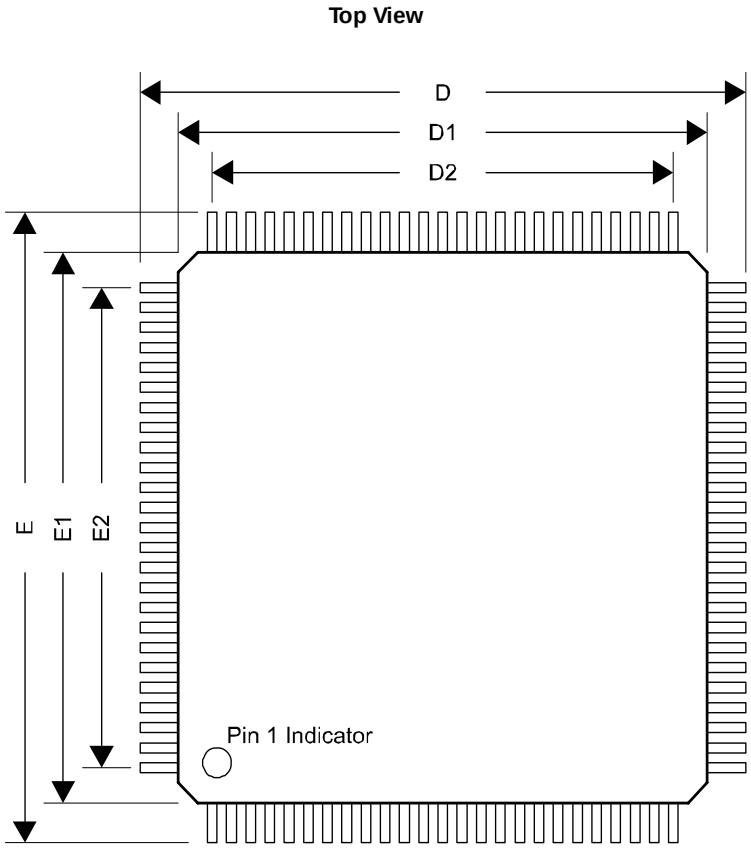
9.4. RoHS Compliance

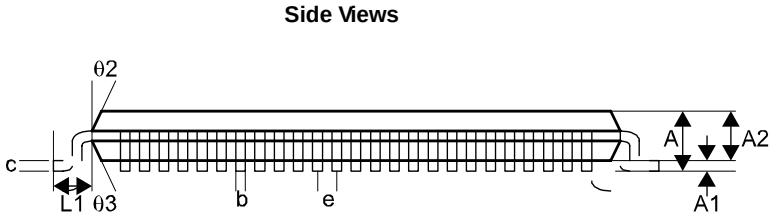
INT5500 is designated to be "Lead-free" and comply with the requirements of the European Union's Restriction on Use of Hazardous Substances (ROHS).

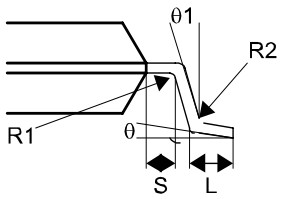
Intellon certifies that the INT5500IC is compatible with the current RoHS requirements for the substances listed below:

Substance	Specification
Lead	< 1000 ppm
Mercury	< 1000 ppm
Cadmium	< 100 ppm
Hexavalent Chromium	< 1000 ppm
Poly Brominated Biphenyls	< 1000 ppm
Poly Brominated Diphenyl Ethers	< 1000 ppm

9.5. Physical Specifications







Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	16.00 BSC.		
D1	14.00 BSC.		
D2	12.00		
E	16.00 BSC.		
E1	14.00 BSC.		
E2	12.00		
R2	0.06	-	0.20
R1	0.08	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	-	-
b	0.17	0.20	0.27
e	0.50 BSC.		

10. Switching Characteristics

10.1. System Clock and Reset Timing

System Clock and Reset Timing

Symbol	Parameter	Min	Typ	Max	Units
50 MHz Master CLK Reference					
t_{CLKp}	CLK period	20 - 25 ppm	20	20 + 25 ppm	ns
t_{CLKhi}	CLK high time	18	20	22	ns
t_{CLKlo}	CLK low time	18	20	22	ns
Reset Timing					
t_{RSTa}	RESET_N active time	200			ms

Note: t_{RSTa} is measured from Power and Clock (XIN_50) both stable.
RST has no synchronous relationship to Clock.

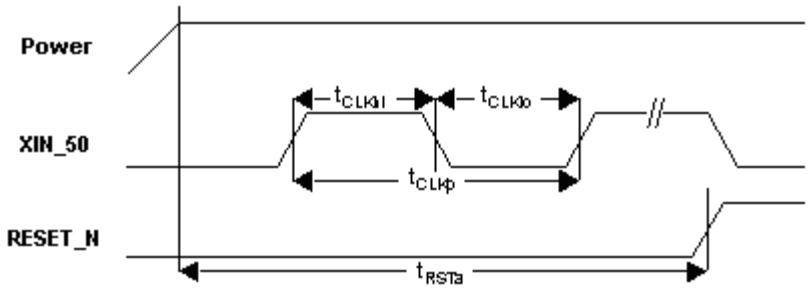


Figure 11: System Clock and Reset Timing

10.2. Analog Front End Interface Timing

AFE Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{AFEp}	AFE_CLK period	40 - 25 ppm	40	40 + 25 ppm	ns
t_{AFEhi}	AFE_CLK high time	18		22	ns
t_{AFElo}	AFE_CLK low time	18		22	ns
t_{ATXp}	ATX_CLK period	10 - 25 ppm	10	10 + 25 ppm	ns
t_{ATXhi}	ATX_CLK high time	4.5		5.5	ns
t_{ATXlo}	ATX_CLK low time	4.5		5.5	ns
t_{ATXi}	ATX_CLK to ATX_DATA, ATX_SYNC, ATX_MODE, ATX_EN invalid	2.0			ns
t_{ATXv}	ATX_CLK to ATX_DATA, ATX_SYNC, ATX_MODE, ATX_EN valid			5.5	ns
t_{ARXp}	ARX_CLK period	10 - 25 ppm	10	10 + 25 ppm	ns
t_{ARXhi}	ARX_CLK high time	4.5		5.5	ns
t_{ARXlo}	ARX_CLK low time	4.5		5.5	ns
t_{ARXsu}	ARX_DATA, ARX_SYNC to ARX_CLK setup	2.0			ns
t_{ARXho}	ARX_DATA, ARX_SYNC to ARX_CLK hold	0.25			ns
t_{ASCp}	ASC_CLK period	200			ns
t_{ASChi}	ASC_CLK high time	100			ns
t_{ASClo}	ASC_CLK low time	100			ns
t_{ASCi}	ASC_CLK to ASC_DATA, ASC_EN invalid	50			ns
t_{ASCv}	ASC_DATA, ASC_EN valid to ASC_CLK	50			ns
t_{ASCsu}	ASC_DATA to ASC_CLK setup	25			ns
t_{ASCho}	ASC_DATA to ASC_CLK hold	0			ns

Note: ASC_CLK is a non-continuous clock that may be stopped high or low for varying periods of time. AFE_PWRDN is not synchronous to any clock.

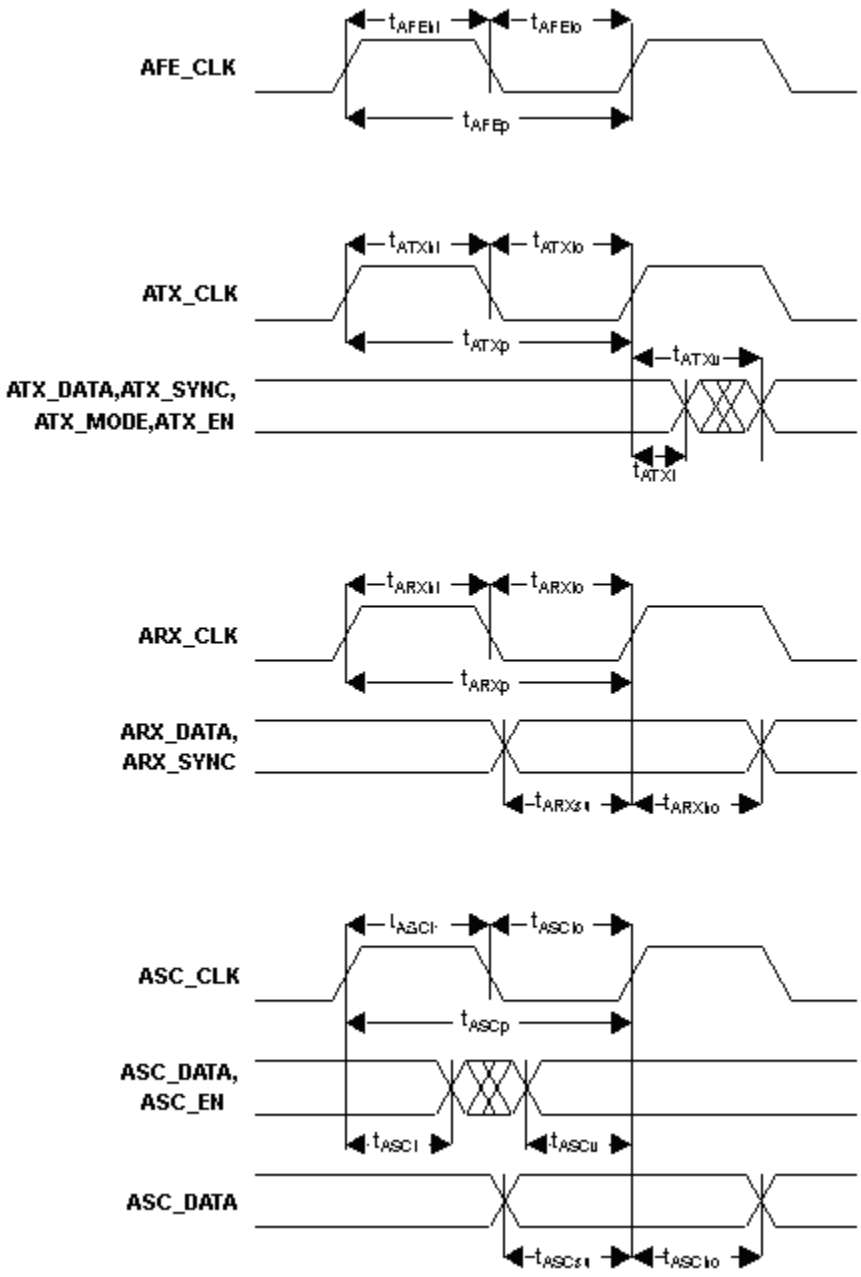


Figure 12: Analog Front End Interface Timing

10.3. MII Timing

MII Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{MIIp}	MTX_CLK, MRX_CLK period (100 mb/s, 10 mb/s)		40/400		ns
t_{MIIhi}	MTX_CLK, MRX_CLK high time (100 mb/s, 10 mb/s)	14/140	20/200	26/260	ns
t_{MIIlo}	MTX_CLK, MRX_CLK low time (100 mb/s, 10 mb/s)	14/140	20/200	26/260	ns
t_{MIIi}	MTX_CLK to TXD, TX_EN, TX_ER invalid	10			ns
t_{MIIv}	MTX_CLK to TXD, TX_EN, TX_ER valid			25	ns
t_{MIIsu}	RXD, RX_DV, RX_ER to MRX_CLK setup	10			ns
t_{MIIho}	RXD, RX_DV, RX_ER to MRX_CLK hold	10			ns
t_{MDp}	MDC period		600		ns
t_{MDhi}	MDC high time		300		ns
t_{MDlo}	MDC low time		300		ns
t_{MDi}	MDC to MDIO invalid	0			ns
t_{MDv}	MDC to MDIO valid			300	ns
t_{MDsu}	MDIO to MDC setup	10			ns
t_{MDho}	MDIO to MDC hold	10			ns

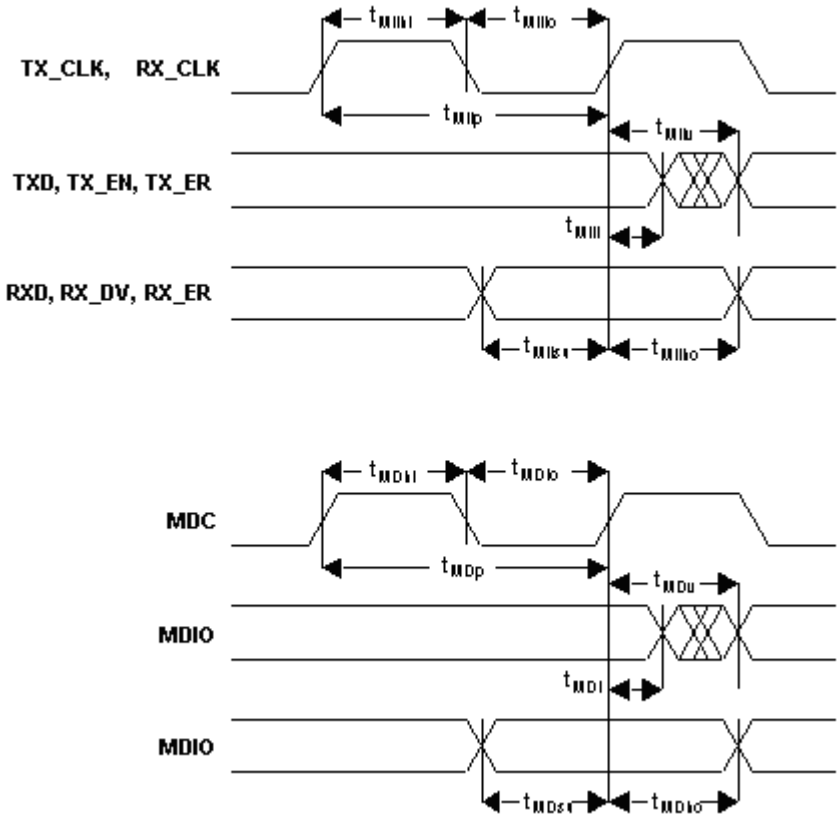


Figure 13: MII Timing

10.4. Non-Volatile Memory Interface Timing

NVM Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{EEp}	SPI_CLK period		480		ns
t_{EEhi}	SPI_CLK high time		240		ns
t_{EElo}	SPI_CLK low time		240		ns
t_{EEi}	SPI_CLK falling to SPI_DO invalid	0			ns
t_{EEv}	SPI_DO valid to SPI_CLK rising	100			ns
t_{EEsu}	SPI_DI to SPI_CLK rising setup	20			ns
t_{EEho}	SPI_DI to SPI_CLK rising hold	20			ns

Note: SPI_CLK is a non-continuous clock that may be stopped high for varying periods of time. Assertion and de-assertion of SPI_CS is done while SPI_CLK is stopped and has no direct timing relationship with SPI_CLK.

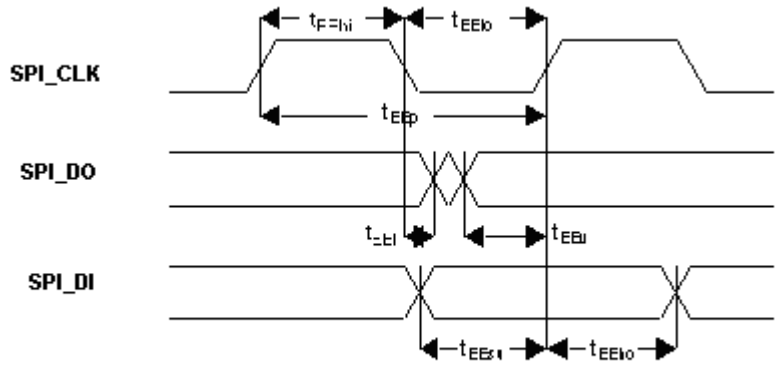
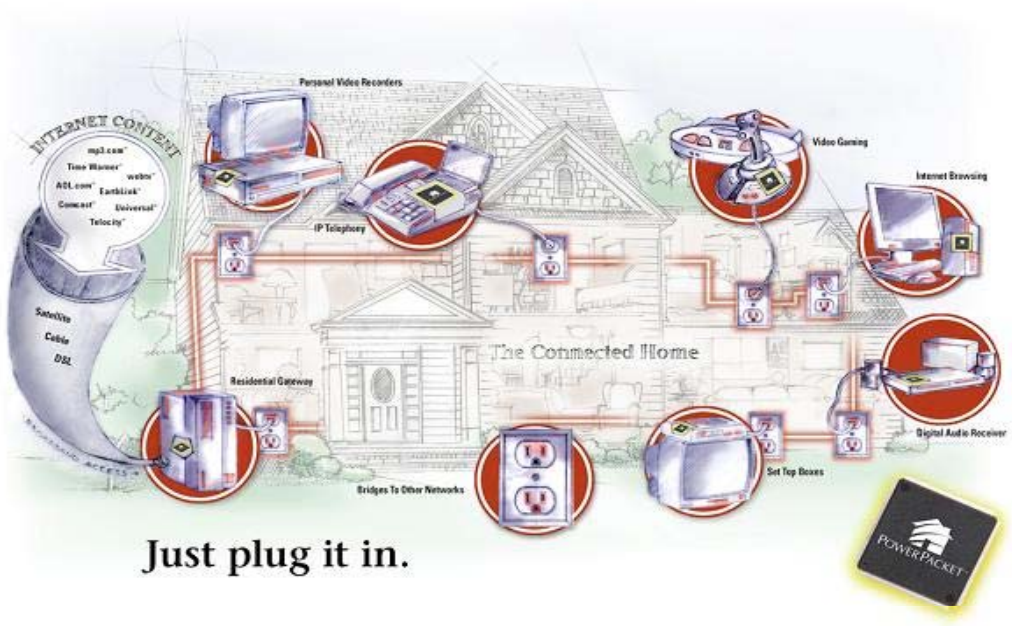


Figure 14: Non-Volatile Memory Interface Timing

11. Revision History

Sections	Description of changes	Revision
All	Original Issue	1.0
Section 8	Addition of MMEs	2.0
Section 8 and 9	Addition of Thermal and RoHS compliance specifications Addition of MMEs	3.0



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