TECHNICAL DATA SHEET

INT1200

Intellon Turbo Analog Front End IC

Features

- Low Power 2.5V CMOS mixed-signal front-end optimized specifically for high speed home network communications
- Direct connection to Intellon INT5500 Turbo Powerline MAC/ PHY transceiver
- High Performance 10-Bit Pipelined ADC
- High Performance current steering 8-bit DAC with adjustable full-scale output current
- Serial configuration interface
- Generation of 2.5V reference voltage from a 3.3V supply through a Voltage Regulator
- -6 dB to 30 dB Low Noise PGA
- Configurable PLL with separate RX and TX output clocks
- 48-pin LQFP

Applications

- Powerline USB adapters
- Powerline to Ethernet bridges and Access Points
- Powerline PCI NICs
- Standard Video TV (SDTV) Distribution
- TV over IP (IPTV)
- DSL/cable modems
- Residential Gateways
- Multi-room audio and set-top boxes
- MP3 jukeboxes
- VoIP telephones
- Game consoles

CONTENTS

1. General Description

Designed specifically for turbo powerline applications, the INT1200 Analog Front End IC provides the subsystem integration required for today's cost-sensitive, high performance communication systems. The INT1200 incorporates a 10 bit analog-to-digital converter and an 8 bit digital-to-analog converter in a single 48-pin LQFP package. The A/D and D/A converters feature a sample rate of 50 and 100 MSPS respectively.

The INT1200 transmitter contains a TX DeMux input port, Interpolation filter and DAC while the receiver contains a PGA, ADC, High Pass Filter, and Receive Mux Output Port.

The low power INT1200 IC is fabricated in an advanced CMOS process. The device is available in a 48-pin LQFP and is specified for operation from 0 to 70 ^{0}C.

Intellon offers a complete solution for powerline communication applications by providing the INT1200 in conjunction with the INT5500 turbo powerline MAC/ PHY IC.

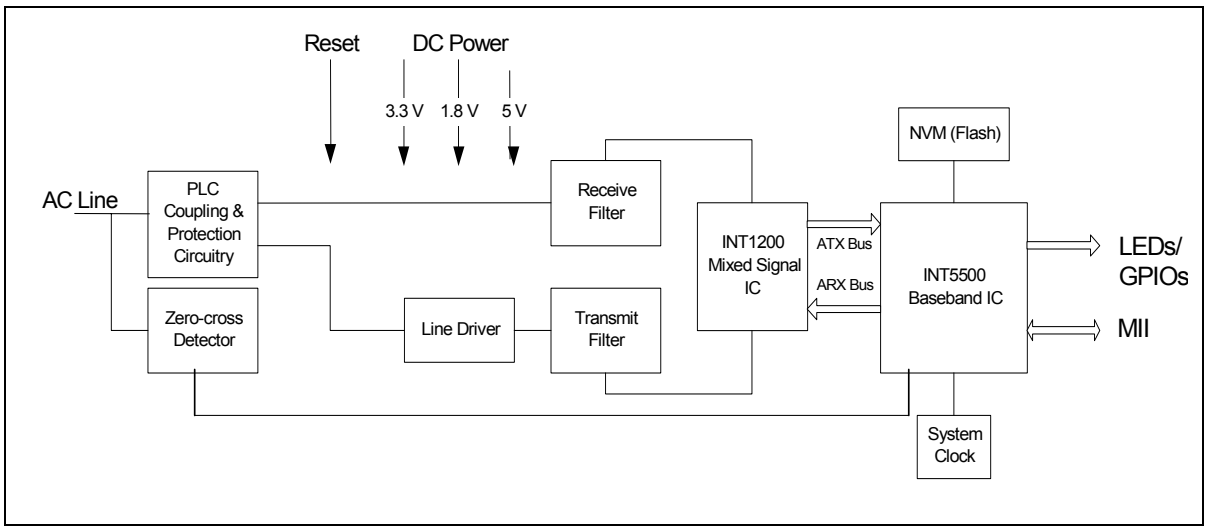


Figure 1. A General System Block Diagram of an INT5500CS (INT1200+INT5500) Based HomePlug Device

2. Master Pin Diagram

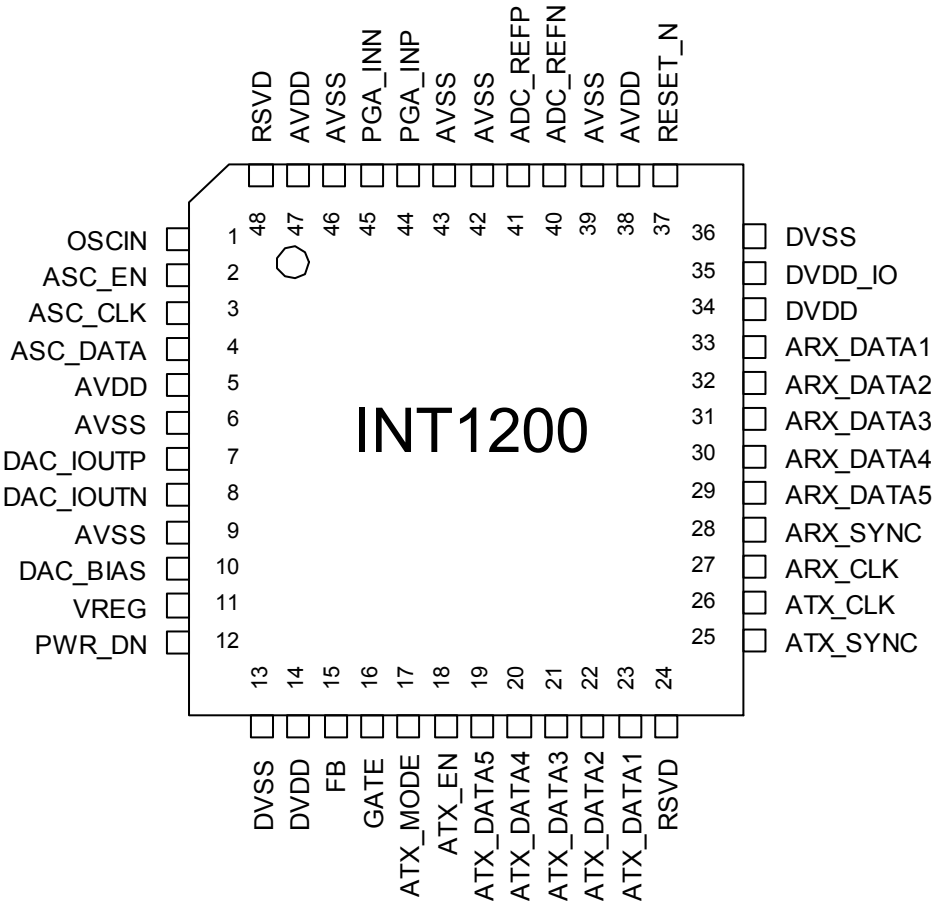


Figure 2. INT1200 IC Master Pin Diagram

3. Master Pin I/O

Pin No.	Signal	Pin No.	Signal
1	**OSCIN**	25	**ATX_SYNC**
2	**ASC_EN**	26	**ATX_CLK**
3	**ASC_CLK**	27	**ARX_CLK**
4	**ASC_DATA**	28	**ARX_SYNC**
5	**AVDD**	29	**ARX_DATA5**
6	**AVSS**	30	**ARX_DATA4**
7	**DAC_IOUTP**	31	**ARX_DATA3**
8	**DAC_IOUTN**	32	**ARX_DATA2**
9	**AVSS**	33	**ARX_DATA1**
10	**DAC_BIAS**	34	**DVDD**
11	**VREG**	35	**DVDD_IO**
12	**PWR_DN**	36	**DVSS**
13	**DVSS**	37	**RESET_N**
14	**DVDD**	38	**AVDD**
15	**FB**	39	**AVSS**
16	**GATE**	40	**ADC_REFN**
17	**ATX_MODE**	41	**ADC_REFP**
18	**ATX_EN**	42	**AVSS**
19	**ATX_DATA5**	43	**AVSS**
20	**ATX_DATA4**	44	**PGA_INP**
21	**ATX_DATA3**	45	**PGA_INN**
22	**ATX_DATA2**	46	**AVSS**
23	**ATX_DATA1**	47	**AVDD**
24	**RSVD**	48	**RSVD**

4. Pin Description

Pin No.	Signal	I/O	Description
1	**OSCIN**	I	25/50 MHz Clock Source Input.
2	**ASC_EN**	I	Serial Bus Enable Input.
3	**ASC_CLK**	I	Serial Clock Input
4	**ASC_DATA**	I/O	Serial Bus Data
5	**AVDD**	I	2.5V Analog Power Supply
6	**AVSS**	I	Analog Ground
7	**DAC_IOUTP**	O	DAC non-inverted differential output current
8	**DAC_IOUTN**	O	DAC inverted differential output current
9	**AVSS**	I	Analog Ground
10	**DAC_BIAS**	I	DAC Output Current adjusts through an external resistor
11	**VREG**	I	Voltage Regulator Control Pin
12	**PWR_DN**	I	Power Down Input. Connect to INT5500 AFE_PWRDN.
13	**DVSS**	I	Digital Ground
14	**DVDD**	I	2.5V Digital Power Supply
15	**FB**	I	Regulator Feedback
16	**GATE**	O	Regulator Output to External Transistor
17	**ATX_MODE**	I	TX Bus Mode Select
18	**ATX_EN**	I	Input Signal to Enable/ Disable Transmit Block
19	**ATX_DATA5**	I	TX Data/ Gain Word Bus Input.
20	**ATX_DATA4**	I	
21	**ATX_DATA3**	I	
22	**ATX_DATA2**	I	
23	**ATX_DATA1**	I	
24	**RSVD**	I	Reserved. Connect to Digital Ground.
25	**ATX_SYNC**	I	Receive Data Synchronization Strobe Input
26	**ATX_CLK**	O	100 MHz PLL Clock Output
27	**ARX_CLK**	O	100 MHz PLL Clock Output
28	**ARX_SYNC**	O	Transmit Synchronization Strobe Output
29	**ARX_DATA5**	O	Receive Data Output Bus.
30	**ARX_DATA4**	O	
31	**ARX_DATA3**	O	
32	**ARX_DATA2**	O	
33	**ARX_DATA1**	O	
34	**DVDD**	I	2.5V Digital Power Supply
35	**DVDD_IO**	I	2.5/3.3V Digital Power Supply
36	**DVSS**	I	Digital Ground
37	**RESET_N**	I	Hardware Reset Input
38	**AVDD**	I	2.5V Analog Power Supply
39	**AVSS**	I	Analog Ground
40	**ADC_REFN**	I	ADC Reference Decoupling Node.
41	**ADC_REFP**	I	
42	**AVSS**	I	Analog Ground
43	**AVSS**	I	Analog Ground
44	**PGA_INP**	I	ADC Non-Inverted Differential Input Voltage
45	**PGA_INN**	I	ADC Inverted Differential Input Voltage
46	**AVSS**	I	Analog Ground
47	**AVDD**	I	2.5V Analog Power Supply
48	**RSVD**	I	Reserved. Connect to Digital Ground.

5. Functional Description

The INT1200 Front End IC connects to INT5500 MAC/PHY IC. The HomePlug MAC/PHY configures and manages the INT1200 via serial interface registers.

5.1. Transmit Path

The INT1200 transmitter contains a TX DeMux Input Port, Interpolation Filter and DAC. The clocks to the transmitter are generated from the internal PLL.

5.1.1. TX DeMux Input Port

The TX DeMux Input Port accepts either a 4-bit data nibble or a 5-bit Gain Control Word depending on the state of the ATX_MODE and ATX_SYNC inputs. The data is sampled on the rising edge of ATX_CLK and in the case of data is demultiplexed into an 8-bit word and sent to the Interpolator. The format of the data nibble is 2's complement. The TX interface port can also accept gain control words in straight binary to be sent to the Gain Control Word Register.

5.1.2. Interpolation Filter

The interpolation filter is designed to run at 100 MHz. The Interpolator accepts 8-bit, 50 MSPS data from the TX interface port and outputs up-sampled/filtered 8-bit data to the DAC at 100 MSPS. The contents of the interpolator are not cleared by any reset signal and therefore, it should be flushed with zeroes before transmitting data. The interpolation can be bypassed by setting a bit in the register bank. The interpolation filter can also enter a test mode where the transmit data is high-pass filtered.

5.1.3. DAC

The INT1200 incorporates a current steering DAC with differential output currents. The DAC accepts 8-bit, 100 MSPS data from the interpolator and outputs differential output currents on DAC_IOUTP and DAC_IOUTN pins. The output currents are designed to drive 25 Ω loads with a compliance range of 500 mV on each output (1 V_{ppd}). For best performance, a full-scale output current of 20 mA should be used (DAC_BIAS resistor = 1.3 kΩ).

The full-scale current is related to the DAC_BIAS resistor by the following equation.

$$I_{out\_total} = \frac{V_{dac\_bias} \times 16}{R_{bias}}$$

5.2. Receive Path

The INT1200 receiver contains a PGA, ADC, High Pass Filter and Receive Mux Output Port. The clocks for the receiver are generated from the internal PLL.

5.2.1. PGA

The PGA has a programmable gain range from -6 dB to +30 dB in 2 dB steps. The input voltage range of 4 V_{ppd} and the maximum full-scale output voltage of the PGA is 2 V_{ppd}. The PGA outputs a differential voltage that is passed to the ADC. The input impedance of the PGA is measured as 250 Ω differentially. The PGA's input is designed to be self-biased to allow for AC coupling in order to minimize offset voltage effects. The PGA includes a decode logic block which accepts the 5-bit Gain Control Word from the register bank and applies the correct gain setting. The register bank can be programmed from either the register interface or the TX bus interface.

5.2.2. ADC

The INT1200 receiver contains a 10-bit, 50 MSPS pipelined ADC which accepts its input signals from the differential PGA output. The full-scale input into the ADC is defined as the maximum output of the PGA. The ADC outputs 10-bit straight binary data as well as an overflow flag to the Digital High Pass Filter and then on to the Receive Mux Output Port.

5.2.3. Digital High Pass Filter

The INT1200 receiver contains a digital receive filter which accepts input signals from the ADC. The purpose of this filter is to remove any residual DC bias. The transfer function is approximately:

$$H(z) = \frac{(Z - 0.99994)}{(Z - 0.98466)}$$

5.3. Receive Output Port

The Receive Output Port accepts 10-bit straight binary data from the Digital High Pass Filter and multiplexes it into 5-bit 2's complement nibbles.

5.4. Clock Generation Port

The clock generation block incorporates a fully integrated PLL. The PLL is capable of accepting either a 25 MHz or a 50 MHz signal from a direct clock input. The clock generation block generates all the required clocks for both the TX and RX paths. The clock generation block outputs a 100 MHz clock as well as a 50 MHz clock. In half-rate receive path mode, the RX clocks are further divided by two so that the RX path runs at 25 MHz.

5.5. VREF Regulator Controller

The INT1200 operates as a mixed 2.5/3.3 V device. To facilitate integration, a 2.5 V reference voltage controller is available. This enables the INT1200 to generate its own 2.5 V supply from a single 3.3 V supply. The controller requires a single external transistor to complete the reference circuit.

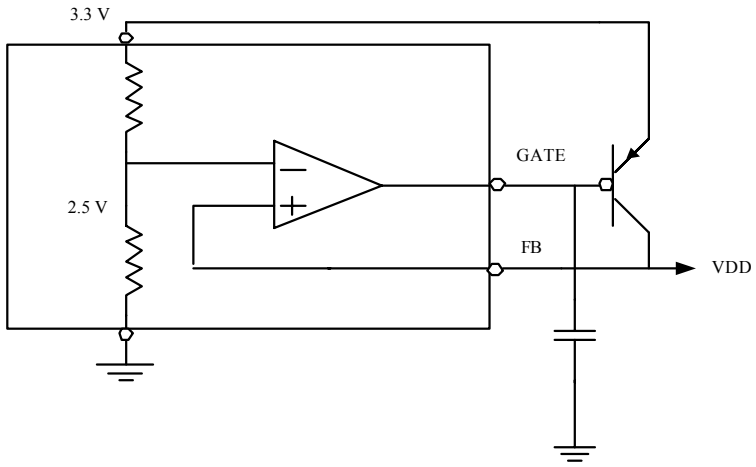


Figure 3. Voltage Regulator

6. Specifications

6.2. Electrical Specifications

6.2.1. Absolute Maximum Ratings

Operation at or above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to these conditions for extended periods of time may affect long-term device reliability. Correct functional behavior is not implied or guaranteed when operating at or above the Absolute Maximum Ratings.

Table 1. Absolute Maximum Ratings for INT1200 IC

Symbol	Parameter	Min	Typ	Max	Units
DVDDIO	Power Supply			+3.63	V
DVDD/AVDD	Power Supply			+2.75	V
	Digital Output Current			5	mA
	Digital Inputs	-0.3		DVDDIO +0.3	V
	Analog Inputs	-0.3		DVDD/AVDD +0.3	V
	Operating Temperature	0		70	^{o}C
	Maximum Junction Temperature			+150	^{o}C
	Storage Temperature	-65		+150	^{o}C
	Lead Temperature (Soldering 10 sec)			+300	^{o}C

6.2.2. AC/ DC Characteristics

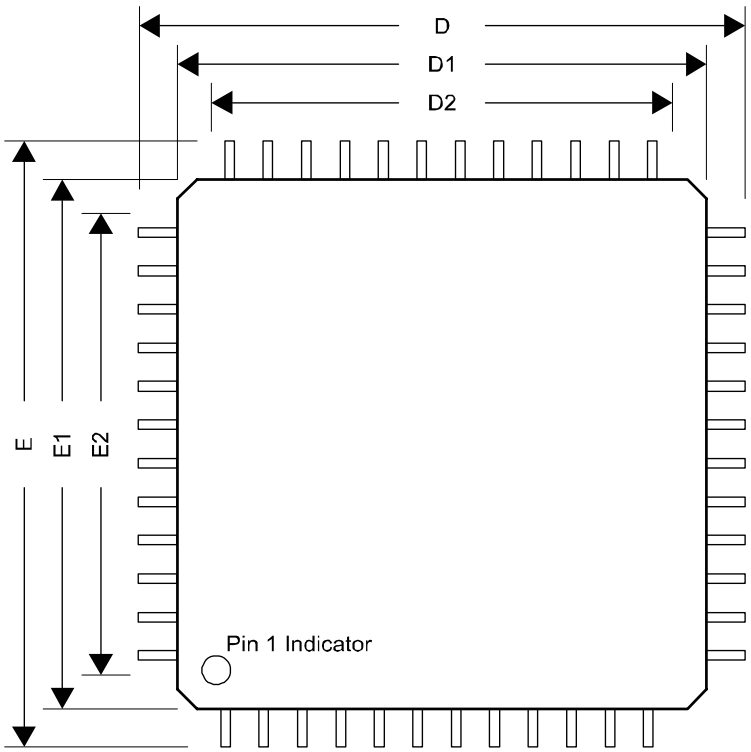
The operating characteristics of the INT1200 are shown in Table 2. for the following operating parameters:
DVDDIO = 3.3 V±10%
AVDD/DVDD = 2.5 V±10%
Gain = -6 dB
f_{oscin} = 25 MHz
R_{bias} = 1.3kΩ
25 Ω DAC load unless otherwise noted

Table 2. INT1200 Specifications

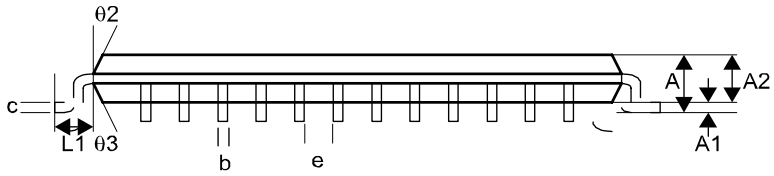
Parameter	Min	Typ	Max	Units
Supply voltage (DVDD/AVDD)	2.25	2.5	2.75	V
DVDD_IO	2.97	3.30	3.63	V
Supply current (Total)		205		mA
Clock Generator Characteristics				
Oscillator in frequency range	12.5	25	50	MHz
Duty cycle	45	50	55	%
Input capacitance		3		pF
Input impedance		100		MW
Input voltage swing		3.30		V
Output voltage swing		3.30		V
DAC				
Supply current		23		mA
Resolution		8		Bits
ENOB	7			Bits
Conversion rate		100		MSPS
Voltage compliance range		0.5		
Full-scale output current	2		20	mA
High Pass Filter				
Cutoff frequency		1.6		MHz
DC rejection		40		dB
ADC				
Supply current		50		mA
Resolution		10		Bits
ENOB	9			Bits
Conversion Rate		50		MSPS
Pipeline delay, ADC clock cycles		6		Cycles
Signal-to-noise ratio		60		dB
Spurious free dynamic range		68		DB
TX/RX Path Interface				
Tx-setup time (t_{su})	2			nS
Tx-hold time (t_{hd})	1			nS
Rx-valid time (t_{vt})			3	nS
Rx-hold time (t_{ht})	2			nS
Power Consumption				
Total current		205		mA
Interpolator		15		mA
DAC		23		mA
PGA		70		mA
ADC		50		mA

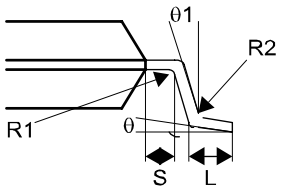
6.3. Physical Specifications

Top View



Side Views





Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	9.00 BSC.		
D1	7.00 BSC.		
D2	5.50		
E	9.00 BSC.		
E1	7.00 BSC.		
E2	5.50		
R2	0.06	-	0.20
R1	0.08	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	-	-
b	0.17	0.20	0.27
e	0.50 BSC.		

7. Timing Information

7.1. Transmit Path Timing

7.1.1. Multiplexed TX Data (ATX_MODE - Low)

The INT1200 expects multiplexed TX data on every rising edge of ATX_SYNC. Two nibbles form a complete 8-bit transmit data sample of 2's complement format. Data is received in 4+4 mode (i.e. the data should appear on pins ATX_DATA[5:2]; ATX_DATA[1] is reserved for Gain Control Word transmission). Transmit data is framed with the TX_SYNC (input) low for the most significant bits followed by TX_SYNC high for the remaining, less significant bits. If TX_SYNC is static low for more than one clock cycle, then zeroes are continuously fed into the transmit data path, independent of the TX[5:2] pins, until TX_SYNC is brought high for the second nibble of a new transmit word. This feature can be used to "flush" the interpolator filters with zeroes.

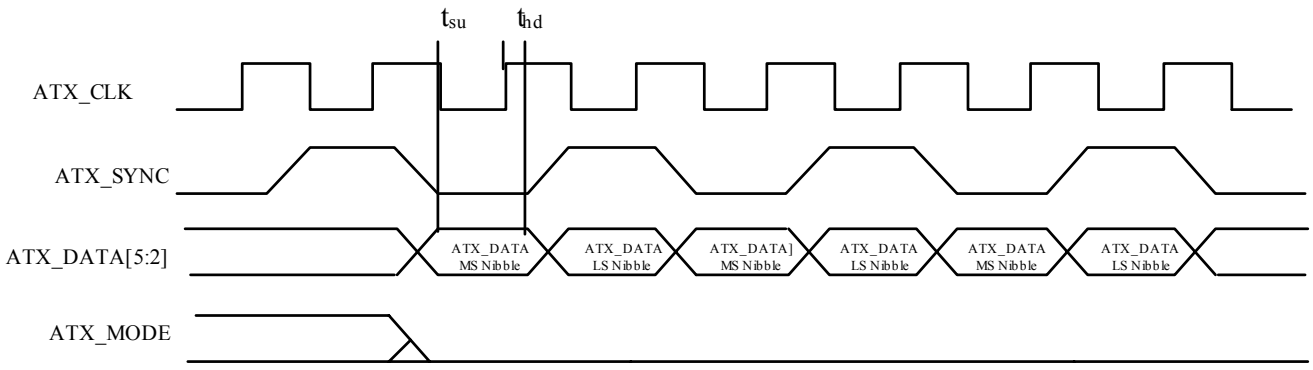


Figure 4. Transmit Path Timing

7.1.2. PGA Gain Setting (ATX_MODE - High)

The INT1200 shares the TX[5:1] pins between transmit data and 5-bit Gain Control Word information for the receive signal Programmable Gain Amplifier (PGA). A high level on the ATX_MODE pin programs the Gain Control Word Register through the TX bus, whereas a low level on the ATX_MODE pin allows data to be fed to the Interpolator. ATX_SYNC must be held low and ATX_MODE must be held high to update the Gain Control Word Register. Furthermore, ATX_SYNC must be held low, ATX_MODE must be held high and the Gain Control Word (ATX_DATA[5:1]) must be stable for at least three clock cycles to update the PGA gain setting.

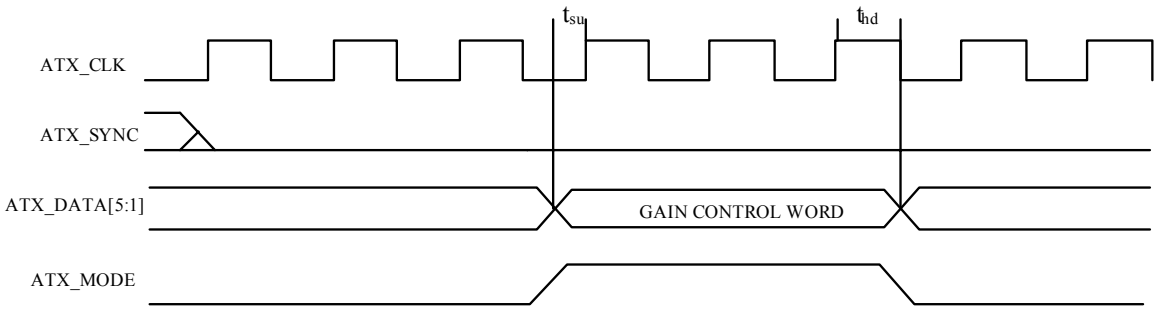


Figure 5. PGA Timing

7.2. Receive Path Timing

7.2.1. Multiplexed RX Data

The INT1200 sends multiplexed data to the RX [5:1] outputs on every rising edge of ARX_CLK. The first nibble of every word is transmitted when RX_SYNC is low. By default, RX_SYNC (output) low frames the most significant bits of the receive data, whereas RX_SYNC is high for the remaining, less significant bits. The ADC is completely read on every second ARX_CLK cycle. Two nibbles form a complete 10-bit receive data sample in 2's complement format.

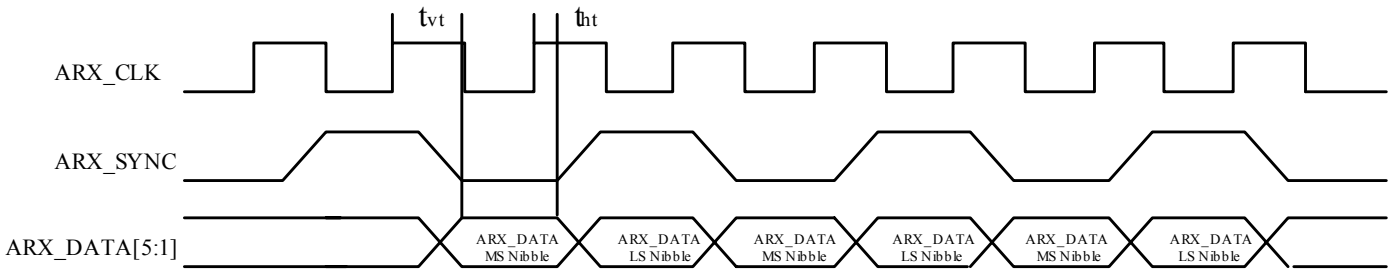
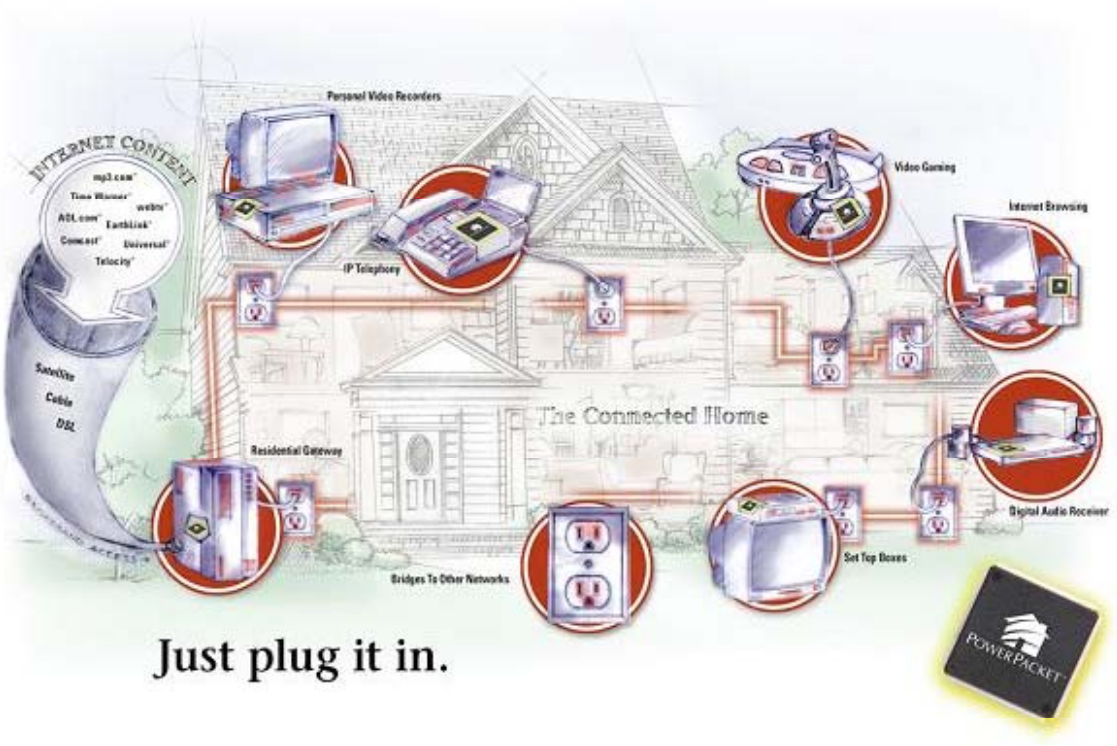


Figure 6. Receive Path Timing

8. Revision History

Sections	Description of changes	Revision
All	Original Issue	1
Figure 1	Updated Figure 1	2



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