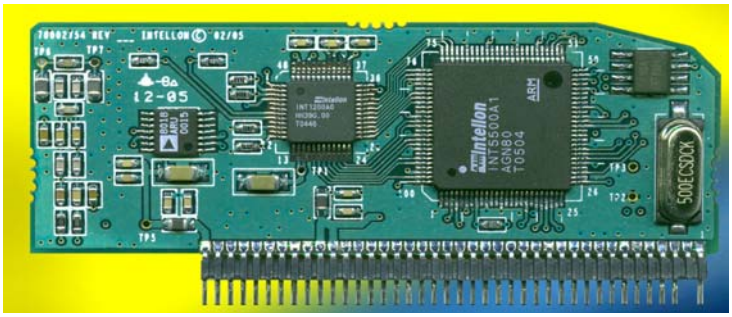
TECHNICAL DATA SHEET

INT55MX

Turbo SIMPLE™ Module

Intellon
NO NEW WIRES.

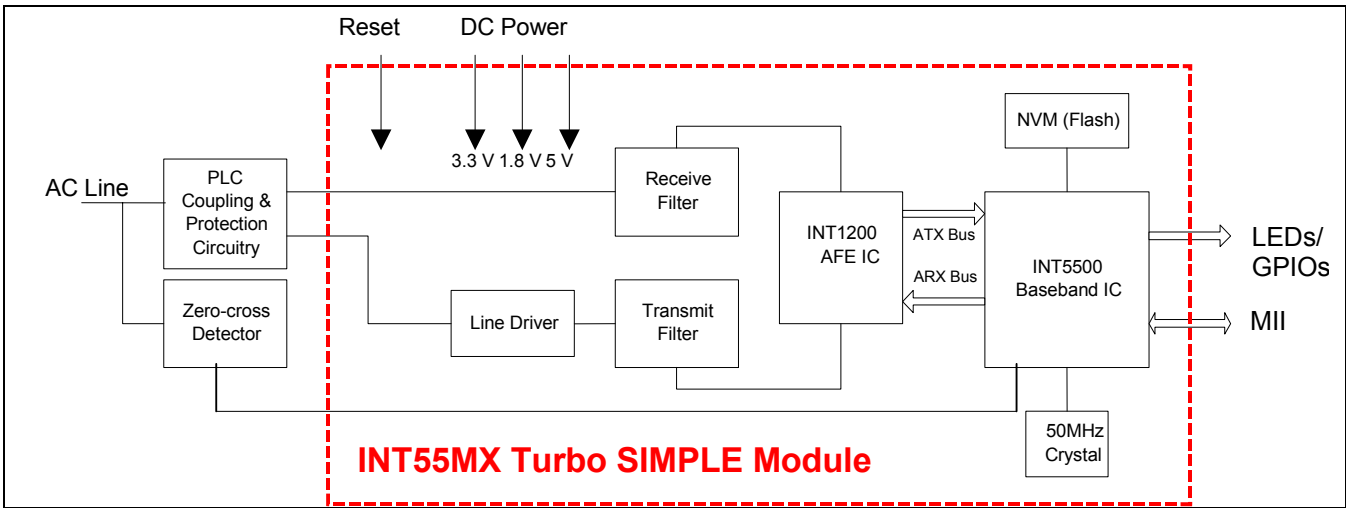


Features

- Based on Intellon's Turbo INT5500CS chipset providing up to 85Mbps data rate on the powerline
- Fully integrated HomePlug™ powerline networking controller with integrated MII (MAC or PHY mode) interfaces
- Fully compatible with the *HomePlug 1.0* standard
- Modular approach with complete collateral allows device manufacturers to buy or build
- Simplifies development cycle, assembly, testing, and certification approvals
- Flash programming via host interface supports ease of manufacture and firmware upgradability
- Upgrade path to future High Speed HomePlug AV SIMPLE modules
- 40-pin low power consumption package

Applications

- Audio and Video distribution
- IPTV Gateways and set-top boxes
- Wall powerline adapters such as Ethernet and Wireless Access Point
- Embedded applications with AC and DC cords such as routers, cable modems, ADSL2+ gateways/ modems, MP3 players and boom boxes
- Broadband Internet, PC file and application sharing
- IP security camera
- Networked gaming
- Expanding the coverage of Wireless LANs



INT55MX Turbo SIMPLE Module Block Diagram

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1. Introduction

Intellon Corporation produces a family of ICs for low-cost, high-speed in-home communications. This family of ICs is supplemented with a line of Single Inline Module devices that incorporate the Intellon Baseband/AFE ICs and required support circuitry to provide a single component solution for the addition of powerline functionality to a product. The SIMPLE ™ (Single Inline Module – Power Line Enabled) family is architected so as Intellon introduces new Baseband and AFE ICs, products incorporating Intellon SIMPLE module can be upgraded to future SIMPLE modules to provide improved performance, functionality and/ or reduced cost with minimum adaptation of existing product designs.

The INT55MX Turbo SIMPLE module is based on the Intellon INT5500 baseband and INT1200 AFE ICs. The host interface to the module is optionally MII PHY for interconnection to microcontrollers or Ethernet controllers or MII Host/DTE for connection to an Ethernet PHY. Spectral shaping of the output signal is optimized for wall-module applications or applications requiring AC/ DC line cord via firmware configuration settings.

The INT55MX SIMPLE module is connected to the host system using Intellon's proprietary SIMPLE PowerBus™ architecture. SIMPLE PowerBus™ provides all the required interface signals between the module and the host system on a single 40-pin connector. This connector allows the module to be easily installed or removed if a socket is used on the host board, or the module may be directly soldered onto the host board for reduced cost. Options are also provided for vertical mount of the module, requiring minimum host board area, or horizontal mount of the module for use in low profile applications.

The INT55MX SIMPLE Module is based on Intellon's turbo chipset, INT5500CS. The module provides two interfaces, via a pin out option:

- **INT55MX (PHY Option):** An MII (IEEE 802.3u 1995, Paragraph 22) PHY interface for interconnection to microcontrollers or Ethernet controllers. The INT55MX (PHY Option) is selected by connecting MODE0 pin to VDD.

- **INT55MX (Host/DTE Option):** An MII Host/DTE interface (IEEE 802.3u 1995, Paragraph 22) for interconnection to an Ethernet PHY. The INT55MX (Host/DTE Option) is selected by connecting MODE0 pin to VSS.

2. INT55MX Simple Module Pin I/O

Pin No.	Pin Name	Pin No.	Pin Name
1	25MHZ	**21**	MII_TXD0
2	KEY	**22**	MII_TXD1
3	VDD_C	**23**	MII_TXD2
4	VSS	**24**	MII_TXD3
5	LINE_SYNC	**25**	VSS
6	MODE0	**26**	PHY_ADRSEL1/ GPIO2*
7	MII_RXD3	**27**	PHY_ADRSEL2/ GPIO3*
8	MII_RXD2	**28**	MII_MDIO
9	MII_RXD1	**29**	MII_MDCLK
10	MII_RXD0	**30**	VDD
11	MII_RXDV	**31**	VDD
12	MII_RXCLK	**32**	RESET_N
13	MII_CRS	**33**	LED2/ GPIO1*
14	MII_RXER	**34**	LED1/ GPIO4*
15	VSS	**35**	VSS
16	GPIO6*	**36**	TX_P
17	MII_TXER	**37**	TX_N
18	MII_TXCLK	**38**	RX_N
19	MII_TXEN	**39**	RX_P
20	MII_COL	**40**	VAA

*** INT5500 GPIO/ LED pins. Refer to INT5500 IC technical data sheet for further details.**

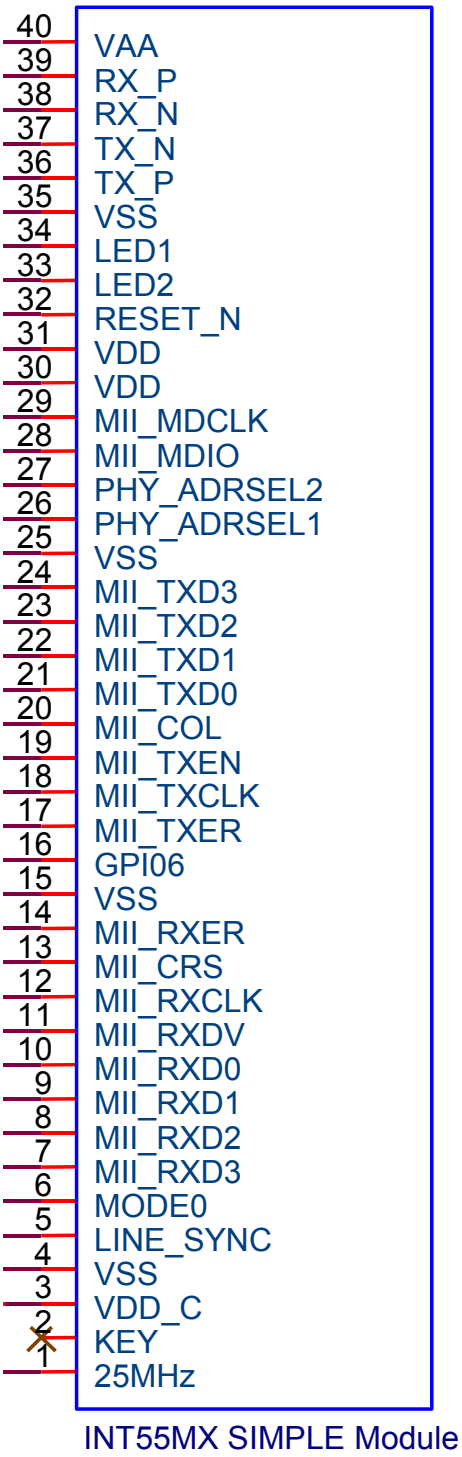


Figure 1. INT55MX Pinout

Notes:

1. Pin 2 is used to key the module connector for proper insertion.

2.1. MII PHY Option

INT55MX SIMPLE Module MII PHY option is selected by connecting the MODE0 to VDD. Following table provides the pin number assignment when INT55MX module is configured for PHY mode.

Pin No.	Pin Name	Function
1	25MHz	25MHz clock output
2	KEY	Unused
3	VDD_C	Core +1.8V DC with respect to ground
4	VSS	Ground Reference
5	LINE_SYNC	AC line zero-cross detect signal
6	MODE0	Mode Select Bit (Tie to VDD for PHY option)
7	MII_RXD3	MII Receive Data bit 3
8	MII_RXD2	MII Receive Data bit 2
9	MII_RXD1	MII Receive Data bit 1
10	MII_RXD0	MII Receive Data bit 0
11	MII_RXDV	MII Receive Data Valid
12	MII_RXCLK	MII Receive Clock
13	MII_CRS	MII Carrier Sense
14	MII_RXER	MII Receive Error
15	VSS	Ground Reference
16	GPIO6	INT5500 IC GPIO6 pin
17	MII_TXER	MII Transmit Error
18	MII_TXCLK	MII Transmit Clock
19	MII_TXEN	MII Transmit Enable
20	MII_COL	MII Collision Detect
21	MII_TXD0	MII Transmit Data Bit 0
22	MII_TXD1	MII Transmit Data Bit 1
23	MII_TXD2	MII Transmit Data Bit 2
24	MII_TXD3	MII Transmit Data Bit 3
25	VSS	Ground Reference
26	PHY_ADRSEL1	MII mgmt address bit 0
27	PHY_ADRSEL2	MII mgmt address bit 1
28	MII_MDIO	MII mgmt data I/ O
29	MII_MDCLK	MII mgmt data clock
30	VDD	+3.3 VDC with respect to ground
31	VDD	+3.3 VDC with respect to ground
32	RESET_N	Resets all Module logic when low
33	LED2	LED Driver Output - Indicates a network link/ activity the PL interface (default setting)
34	LED1	LED Driver Output – indicates Power Good (default setting)
35	VSS	Ground Reference
36	TX_P	Analog Transmit Output to Coupler
37	TX_N	Analog Transmit Output to Coupler
38	RX_N	Analog Receive Input from Coupler
39	RX_P	Analog Receive Input from Coupler
40	VAA	+5V DC with respect to ground

2.2. Pin Descriptions by Group

Group	Pin No	Signal Name	Description	I/O
PHY Option This option is selected when MODE0 is connected to VDD.				
MII	10 9 8 7	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	MII Receive Data Data is transferred from the IC across these four lines one nibble at a time.	O
	12	MII_RXCLK	MII Receive Clock The Receive Clock is synchronous to the data and is continuous. This clock operates at 25 MHz.	O
	11	MII_RXDV	MII Receive Data Valid This Signal indicates that the data on the MII_RXD[3:0] pins are valid.	O
	14	MII_RXER	MII Receive Error The MII_RXER signal indicates that an error has occurred during frame reception.	O
	20	MII_COL	MII Collision Detect The MII Collision Detect Signal indicates to the MAC that a collision has occurred on the MII interface. MII_COL is an asynchronous output signal.	O
	21 22 23 24	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	MII Transmit data Data is transferred to the IC across the four lines one nibble at a time.	I
	18	MII_TXCLK	MII Transmit Clock The Transmit Clock outputs a continuous clock. This clock operates at 25MHz.	O
	19	MII_TXEN	MII Transmit Enable The MII Transmit Enable signal indicates that valid data is present on the MII_TXD[3:0] pins.	I
	13	MII_CRS	MII Carrier Sense The MII Carrier Sense signal is asserted within 30 MII clocks after MII_TXEN indicates a TX frame is being sent by the local host. MII CRS stays true until the entire TX frame is loaded into an internal buffer and a new buffer is allocated to the MII TX interface. This signal should be used monitored by the MII TX host. A new MII TX frame should not be sent until MII CRS returns to false to prevent TX buffer overflows. MII_CRS is an asynchronous output signal.	O
	17	MII_TXER	MII Transmit Error Assertion of this signal causes intentionally bad data to be transmitted. The MII interface will discard any incoming frame received when if this signal is asserted while MII_TXEN is true.	I

Group	Pin No	Signal Name	Description	I/O
	28	MII_MDIO	MII Management Data Input/Output The MII_MDIO signal is a bi-directional data pin for the Management Data Interface (MDI).	I/O
	29	MII_MDCLK	MII Management Data Clock The MII_MDCLK signal is a clock reference for the MII_MDIO signal.	I
	26	PHY_ADRSEL1	Address Select 0 Used to compare against the upper two bits of MDI Address.	I
	27	PHY_ADRSEL2	Address Select 1 Used to compare against the upper two bits of MDI Address.	I
	1	25MHZ	25MHZ Clock Output	O
General Groups				
Control	5	LINE_SYNC	AC line zero-cross detect signal	I
	16	GPIO6	The pull-up/ pull-down values is latched as Boot Source upon power-up/ reset. Tie to VSS for normal operation.	I/O
LEDs	34	LED1	LED Driver Output – Indicates Power Good (default setting)	O
	33	LED2	LED Driver Ouput – Indicates network link/ activity on the PL interface (default setting)	O
Reset	32	RESET_N	Resets all module logic when low	I
AFE	36 37 38 39	TX_P TX_N RX_N RX_P	Analog Transmit Output (Complimentary) Analog Transmit Output Analog Receive Input Analog Receive Input (Complementary)	O O I I
Power & Ground	4,15,25,35	VSS	Ground	I
	30,31	VDD	+3.3V DC with respect to VSS	I
	3	VDD_C	+1.8V DC with respect to Ground	I
	40	VAA	+5V DC with respect to Ground	I
Mode Select	6	MODE0	Mode Select Pin Tie to VDD for PHY option.	I
NC	2	KEY	Unused	

2.3. Host/ DTE Option

INT55MX SIMPLE Module Host/DTE option is selected by connecting the MODE0 to VSS. Following table provides the pin number assignment when INT55MX module is configured for HOST/DTE mode.

Pin No.	Pin Name	Function
1	25MHz	25MHz clock output
2	KEY	Unused
3	VDD_C	Core +1.8V DC with respect to Ground
4	VSS	Ground Reference
5	LINE_SYNC	AC line zero-cross detect signal
6	MODE0	Mode Select Bit (Tie to VSS for Host/ DTE option)
7	MII_RXD3	MII Receive Data bit 3
8	MII_RXD2	MII Receive Data bit 2
9	MII_RXD1	MII Receive Data bit 1
10	MII_RXD0	MII Receive Data bit 0
11	MII_RXDV	MII Receive Data Valid
12	MII_RXCLK	MII Receive Clock
13	MII_CRS	MII Carrier Sense
14	MII_RXER	MII Receive Error
15	VSS	Ground Reference
16	GPIO6	INT5500 IC GPIO6 pin
17	MII_TXER	MII Transmit Error
18	MII_TXCLK	MII Transmit Clock
19	MII_TXEN	MII Transmit Enable
20	MII_COL	MII Collision Detect
21	MII_TXD0	MII Transmit Data Bit 0
22	MII_TXD1	MII Transmit Data Bit 1
23	MII_TXD2	MII Transmit Data Bit 2
24	MII_TXD3	MII Transmit Data Bit 3
25	VSS	Ground Reference
26	GPIO2	Connect to VDD through a 3.3KΩ resistor or lower
27	GPIO3	Connect to VSS through a 3.3KΩ resistor or lower
28	MII_MDIO	MII mgmt data I/ O
29	MII_MDCLK	MII mgmt data clock
30	VDD	+3.3 VDC with respect to ground
31	VDD	+3.3 VDC with respect to ground
32	RESET_N	Resets all Module logic when low
33	LED2	LED Driver Output - Indicates a network link/ activity the PL interface (default setting)
34	LED1	LED Driver Output – indicates Power Good (default setting)
35	VSS	Ground Reference
36	TX_P	Analog Transmit Output to Coupler
37	TX_N	Analog Transmit Output to Coupler
38	RX_N	Analog Receive Input from Coupler
39	RX_P	Analog Receive Input from Coupler
40	VAA	+5V DC with respect to Ground

2.4. Pin Descriptions by Group

Group	Pin No	Signal Name	Description	I/O
HOST/ DTE Option This option is selected when MODE0 is tied to VSS.				
MII	10 9 8 7	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	MII Receive Data Data is transferred from the IC across these four lines one nibble at a time.	I
	12	MII_RXCLK	MII Receive Clock The Receive Clock is synchronous to the incoming data and is continuous. This clock operates at 25 MHz (100BaseT) or 2.5 MHz (10BaseT).	I
	11	MII_RXDV	MII Receive Data Valid This Signal indicates that the data on the MII_RXD[3:0] pins are valid.	I
	14	MII_RXER	MII Receive Error The MII_RXER signal indicates that an error has occurred during frame reception.	I
	20	MII_COL	MII Collision Detect The MII Collision Detect signal indicates that a collision has been detected on the MII interface and shall remain asserted while the collision condition persists.	I
	21 22 23 24	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	MII Transmit data Data is transferred to the IC across the four lines one nibble at a time.	O
	18	MII_TXCLK	MII Transmit Clock This clock operates at 25MHz (100BaseT) or 2.5MHz (10BaseT).	I
	19	MII_TXEN	MII Transmit Enable The MII Transmit Enable signal indicates that valid data is present on the MII_TXD[3:0] pins.	O
	13	MII_CRS	MII Carrier Sense The MII Carrier Sense signal is asserted when either the transmit or receive medium is non-idle.	I
	17	MII_TXER	MII Transmit Error Assertion of this signal causes intentionally bad data to be transmitted.	O
	28	MII_MDIO	MII Management Data Input/Output The MII_MDIO signal is a bi-directional data pin for the Management Data Interface (MDI).	I/O
	29	MII_MDCLK	MII Management Data Clock The MII_MDCLK signal is a clock reference for the MII_MDIO signal.	O

Group	Pin No	Signal Name	Description	I/O
	1	25MHZ	25 MHz clock to Ethernet PHY IC.	O
General Groups				
Control	5	LINE_SYNC	AC line zero-cross detect signal	I
	16	GPIO6	The Pull-up/ Pull –down values is latched as Boot Source upon power-up/ reset. Tie to VSS for normal operation.	I/O
LEDs	34	LED2	LED Driver Output - Indicates a network link/ activity the PL interface (default setting)	O
	33	LED1	LED Driver Output – indicates Power Good (default setting)	O
Reset	32	RESET_N	Resets all module logic when low.	I
AFE	36 37 38 39	TX_P TX_N RX_N RX_P	Analog Transmit Output (Complimentary) Analog Transmit Output Analog Receive Input Analog Receive Input (Complementary)	O O I I
Power & Ground	4,15,25, 27, 35	VSS	Ground	I
	26,30,31	VDD	+3.3V DC with respect to Ground	I
	3	VDD_C	+1.8V DC with respect to Ground	I
	40	VAA	+5V DC with respect to Ground	I
Mode Select	6	MODE0	Mode Select Pin Tie to VSS for PHY option.	I
NC	2	NC	Unused	

3. INT55MX SIMPLE Module Specifications

3.1. Electrical Specifications

Electrical specifications for the INT55MX module are presented in Table 1.

Table 1: Electrical Specifications

Parameter	Min	Typ.	Max	Unit
VDD Supply Voltage	3.0	3.3	3.6	V
VDD Supply Current		285		mA
VDD_C Supply Voltage	1.62	1.8	1.98	V
VDD Supply Current		325		mA
VAA Supply Voltage	4.75	5	8.0	V
VAA Supply Current		25	30	mA

The typical power consumption for the INT55MX SIMPLE module is 1.65W.

3.2. Mechanical Specification

Placement of the INT55MX Module's major component blocks is presented in Figure 2.

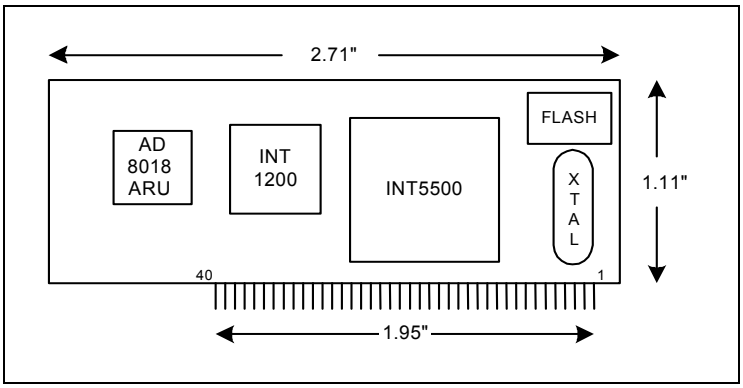


Figure 2: INT55MX SIMPLE Module Component Placement

4. INT55MX SIMPLE Module Design Considerations

4.1. Crystal Considerations

The INT5500 IC on the SIMPLE module requires close clock accuracy for optimum power line performance. A 3rd overtone 50MHz crystal oscillator has been chosen for the module clock source to provide high accuracy at minimum cost. Specifications for the crystal are detailed in Table 2.

Table 2: INT55MX SIMPLE Module Crystal Specification

Parameter	Specification	Units
Mode	3rd Overtone	
Frequency	50.000	MHz
Frequency Tolerance (25°C)	+/-10 (Max)	ppm
Aging and Temperature Tolerance	+/-15 (Max)	ppm
Load Capacitance	18	pF
ESR (Max)	80	Ohm
C0	4.1 – 7 (Max)	pF
Operating Temperature Range	-10 → +70	°C
Storage Temperature	-30 → +85	°C
Case Style	CSM-7 (4.3mm)	
Manufacturer Part Number	**ECS-500-18-5P-CK-TR**	

4.2. Line Driver

The line driver of the INT55MX SIMPLE module is based on the AD8018ARU xDSL line drive amplifier. The amplifier is powered through a filter from the bus +5V supply. Power supply current for the AD8018ARU is approximately 30 mA when transmitting into a 5Ω AC load. The input impedance of the amplifier should be set to 50 ohms so that its matches the output impedance of the transmit filter.

4.3. Non-Volatile Memory

The INT5500 IC on the SIMPLE module provides a serial peripheral interface (SPI) for downloading the run-time MAC software from an on-board flash memory device. The INT5500 acts as a master on the SPI. Flash memory devices appropriate for the INT55MX SIMPLE module are listed in Table 3.

Table 3: Supported Flash Devices

Part Number	Memory Type	Memory Size (bits)	Vendor
M25P10-A	Flash	1 M	STMicroelectronics *

4.4. INT55MX SIMPLE Module On-board Configuration Straps

The INT55MX SIMPLE module uses GPIO pins for LED connections, the power-on state of these GPIO pins must be taken into account when configuring these pins. Refer to the INT5500 Turbo IC technical data sheet for correct LED connections.

4.5. Regulatory Compliance Considerations

Regulatory compliance of PLC products generally covers two areas:

- Safety (UL, CSA, etc.)
- Emissions (FCC Part 15, CE, etc.)

Safety in INT55MX SIMPLE Module designs will typically involve power supply design and PLC coupling circuitry design. If an external power supply /coupler is used, the UL safety requirements will typically only impact the adapter and not the host device. If AC line voltage is brought into the host device, then all UL requirements for the class of host device must be met.

Verification of emissions requirements for INT55MX Module design requires measurement of potential interference from the PLC signal applied to the power line as well as radiated and conducted emissions due to the digital circuitry in the host device. Conformance with the HomePlug PSD mask for the device transmit signal will generally allow the device to meet power line carrier device requirements. Normal care should be exercised in the design and layout of the host device printed circuit board and mechanical design to ensure compliance with radiated and conducted emissions rules.

5. INT55MX SIMPLE Module Connector

The INT55MX module is connected to the host system using Intellon's proprietary SIMPLEPowerBus™ architecture. SIMPLEPowerBus™ utilizes an industry standard header using 0.018" square pins on 0.050" centers. This connector provides for easy insertion and removal of module devices using a mating female header. Alternatively, the device may be soldered directly to the host board.

Connector options are available to allow the INT55MX to be mounted in a vertical orientation or in a horizontal orientation. A right-angle header may be used to mount the module vertically as shown in Figure 3. This module orientation minimizes the host board space require by the module. A straight header may be used to mount the module horizontally as shown in Figure 4. This orientation would be used in applications requiring a low-profile footprint.

Pin 2 of the connector is used as a key for proper orientation of the module. This pin is deleted from the module connector and a "plug" inserted in the female host connector.

Connector part numbers and source for the INT55MX module are listed in Table 4.

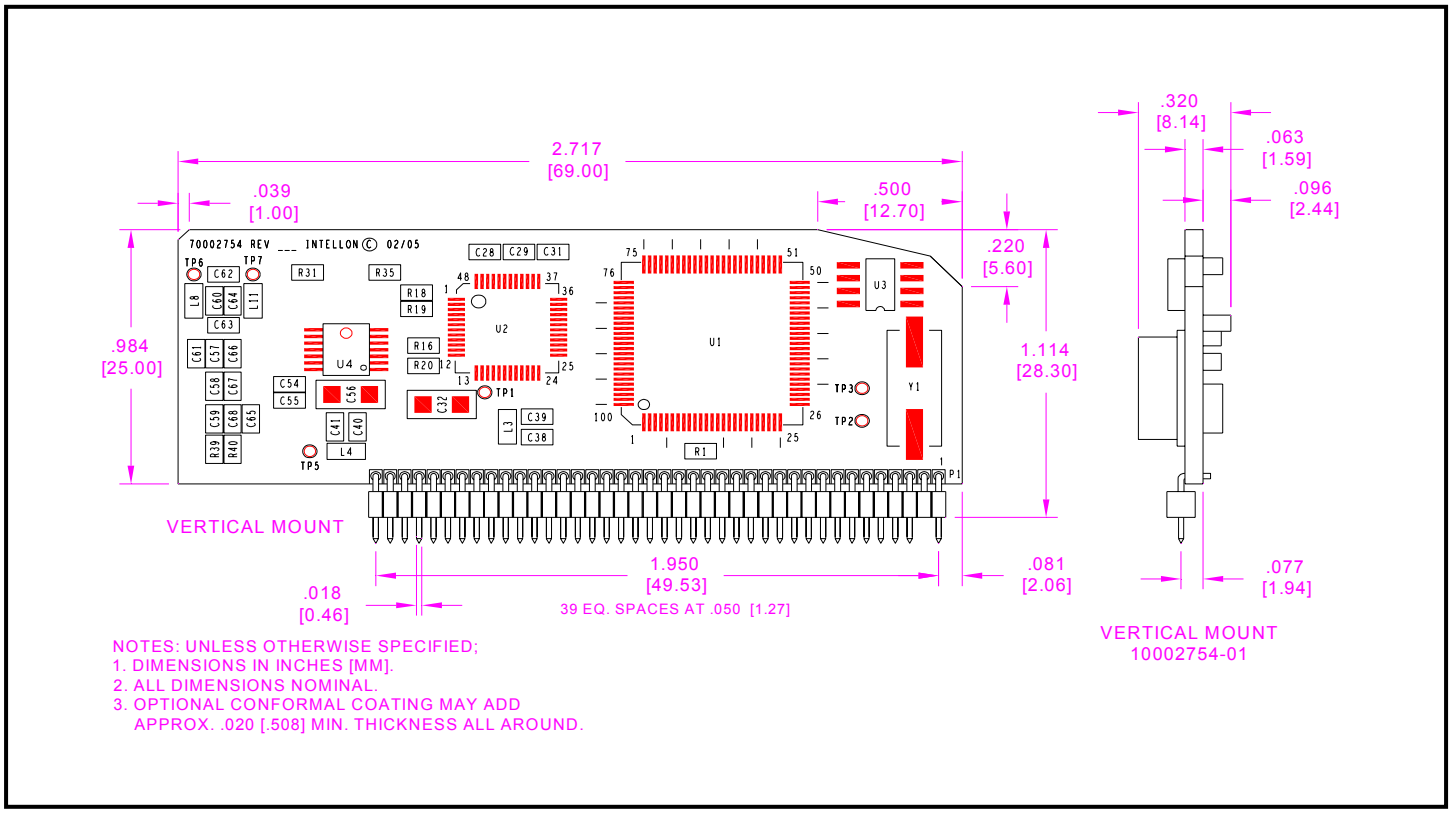


Figure 3: INT55MX Module with Right-Angle Connector

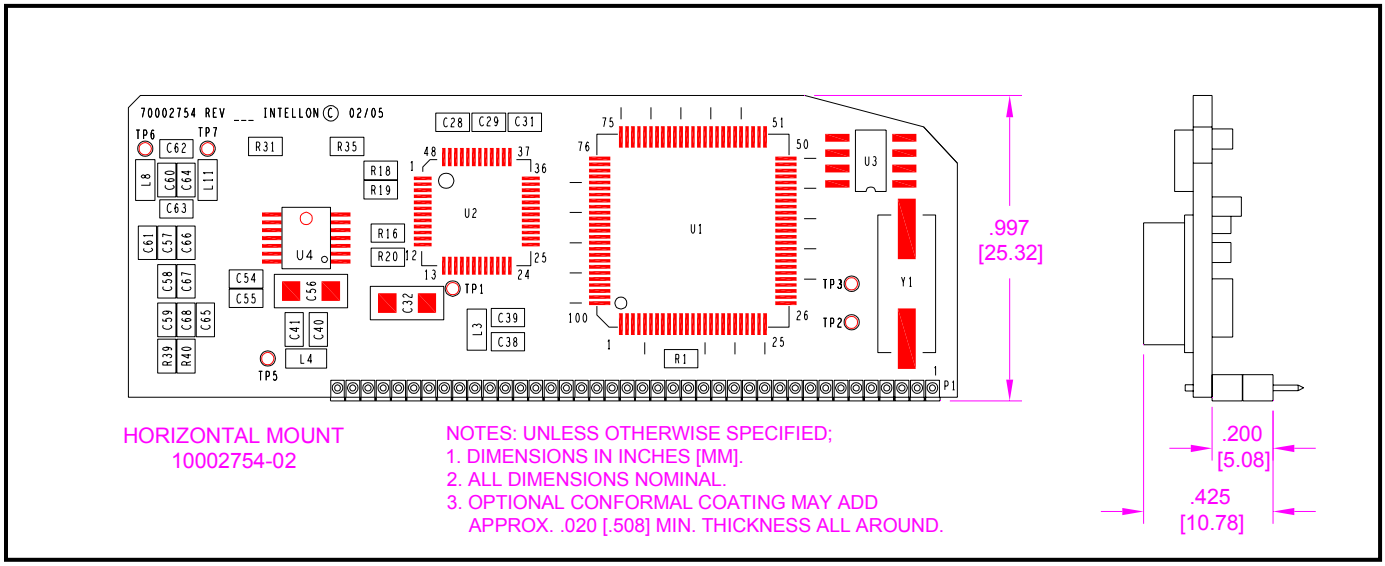


Figure 4: INT55MX Module with Straight Connector

Table 4: SIMPLEPowerBus™ Connector Specification

Connector	Source/Part Number
Female Host Connector	Samtec P/N SLM-140-01-T-S
Host Connector Plug	Samtec P/N TP-12

5.1. INT55MX SIMPLE Module Package Specifications

Table 5 presents basic board specifications for the module PCB.

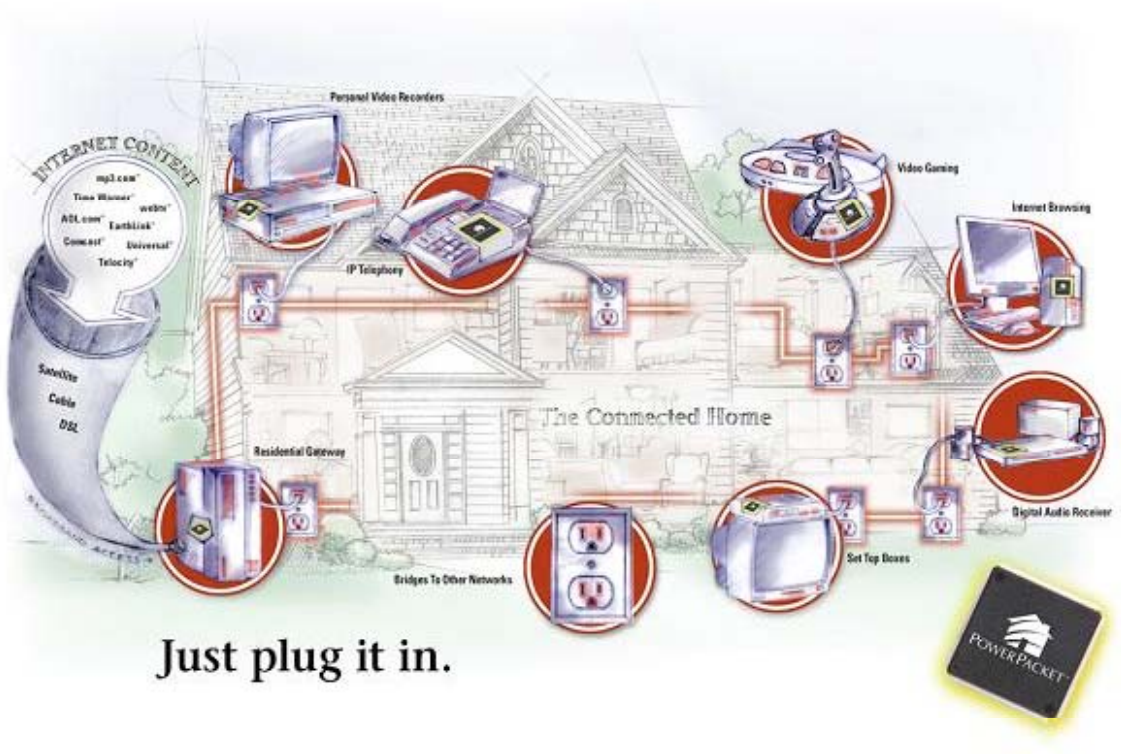
Table 5. INT55MX Module Package Specification

Specification	Value
Board Dimensions	2.71” (l) x 1.11” (h) x 0.35” (w)
Mounting Height (Vertical Mount)	1.2” No Host Connector, 1.3” with Host Connector
Mounting Height (Horizontal Mount)	0.38” No Host Connector, 0.56” with Host Connector

6. Revision History

Table 6: Revision History

Revision	Modifications
1	Advance Release



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