

REVISIONS

REV	DESCRIPTION	CHECKED	DATE	CONF MGMT	DATE
2	ECO #1752 HOLES FOR J1 TIEWRAP				

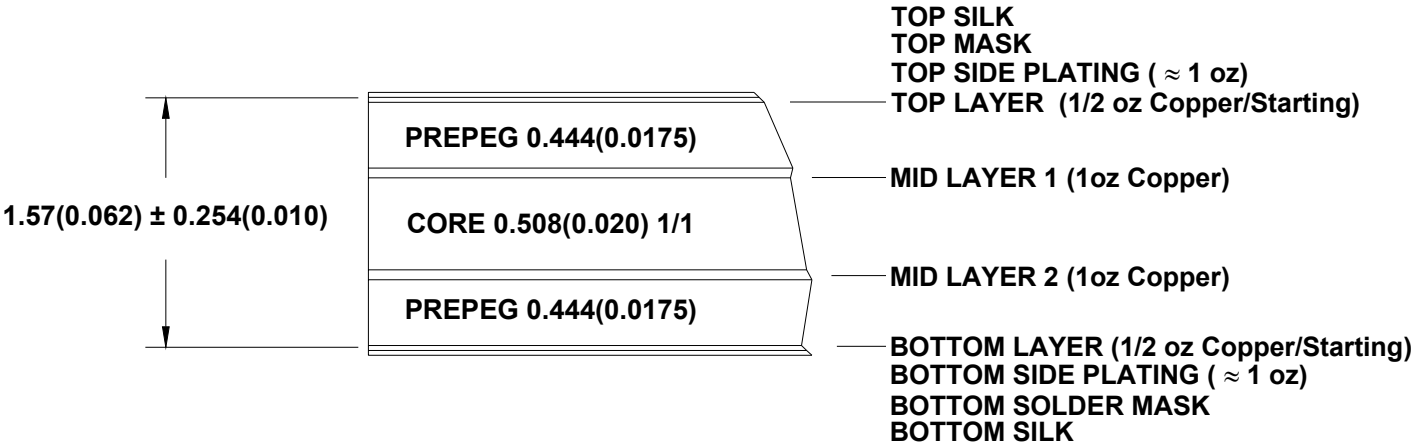
PRINTED CIRCUIT BOARD FABRICATION SPECIFICATION

PCB INFORMATION:	NO: <u>90002755</u> REV: <u>2</u> NAME: <u>RD5500-ETH SIMPLE ADAPTER</u>
GERBER FILES:	FILE: <u>90002755.ZIP</u> FORMAT: <u>5.5, ABS, RS-274-X</u> UNITS: <u>MM(INCH)</u>
DIMENSIONS:	X = <u>151 (5.945)</u> Y = <u>207 (8.150)</u> THICK: <u>1.57 (0.062)</u>
HOLES & VIAS:	TOTAL: <u><2000</u> MIN. DRILL DIA: <u>0.254(0.010)</u> BLIND: <u>0</u> BURIED: <u>0</u> PLUGGED: <u>0</u> DRILL TOLERANCES (<i>WITHIN PAD CENTERS</i>): HOLE DIA > 3.175(0.125) = $\pm 0.127(0.005)$ HOLE DIA $\leq 3.175(0.125)$ = $\pm 0.076(0.003)$
GEOMETRY:	MIN. TRACE: <u>0.100(0.004)</u> MIN. SPACE: <u>0.100(0.004)</u>
LAYERS:	SIGNAL: <u>2</u> PLANES: <u>2</u> TOTAL: <u>4</u> ADD UL ID. SYMBOL AND MFGR WEEK/YEAR MARK TO BOTTOM SIDE COPPER
MATERIAL:	FR4 – NATURAL COLOR, UL94VO
STARTING COPPER:	WEIGHT (oz.) EXTERNAL: <u>0.5</u> INTERNAL: <u>1.0</u> PLANES: <u>N/A</u>
SURFACE FINISH:	1.0 oz. COPPER (.0014 THK.) PLATE OVER FINAL CIRCUIT CONFIGURATION AND ANNULAR WALLS OF PLATED THRU HOLES. ELECTROLESS NICKEL (EN) 50>250uin followed by IMMERSION GOLD 4>12uin. FINISH.
SOLDER MASK:	DARK GREEN LPI (LIQUID PHOTO-IMAGABLE) OVER BARE COPPER
SILK SCREEN:	TOP AND BOTTOM SIDE SILKSCREEN IN WHITE EPOXY INK
NOTES: <u>0.254(0.010) drilled holes are drilled to fill, TOLERANCE +0.025(0.001), -0.229(0.009).</u>	

		ORIGINAL ISSUE APPROVAL			 INTELLON CORPORATION 5100 W. SILVER SPRINGS BLVD. OCALA, FL 34482 PH: (352) 237-7416 FAX: (352) 237-7616 http://www.intellon.com	
		APPROVALS		DATE		
		DRAWN:	TWW	3/15/05		
		CHECKED:				
		APPROVED:				
		CONF MGMT:			FABRICATION SPECIFICATION RD5500-ETH SIMPLE ADAPTER PCB	
	10002755	UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: +/- 1/64 DECIMALS: .XX = +/- .01 .XXX = +/- .003 ANGLES: +/- 1/2°				
NEXT ASSY	USED ON					
APPLICATION						
		SIZE:	FSCM NO:	DWG NO:	80002755	REV:
		A				2
		SCALE: NONE			SHEET: 1 OF 3	
APPROVED "A" SIZE PCB FAB SPEC REVISION: D DATE: 9/9/98 CHANGED BY: G. LASBY REASON FOR CHANGE: NEW LOGO & SIGN OFF						

REVISIONS	
REV	DESCRIPTION
⇒	SEE SHEET 1 FOR REVISION

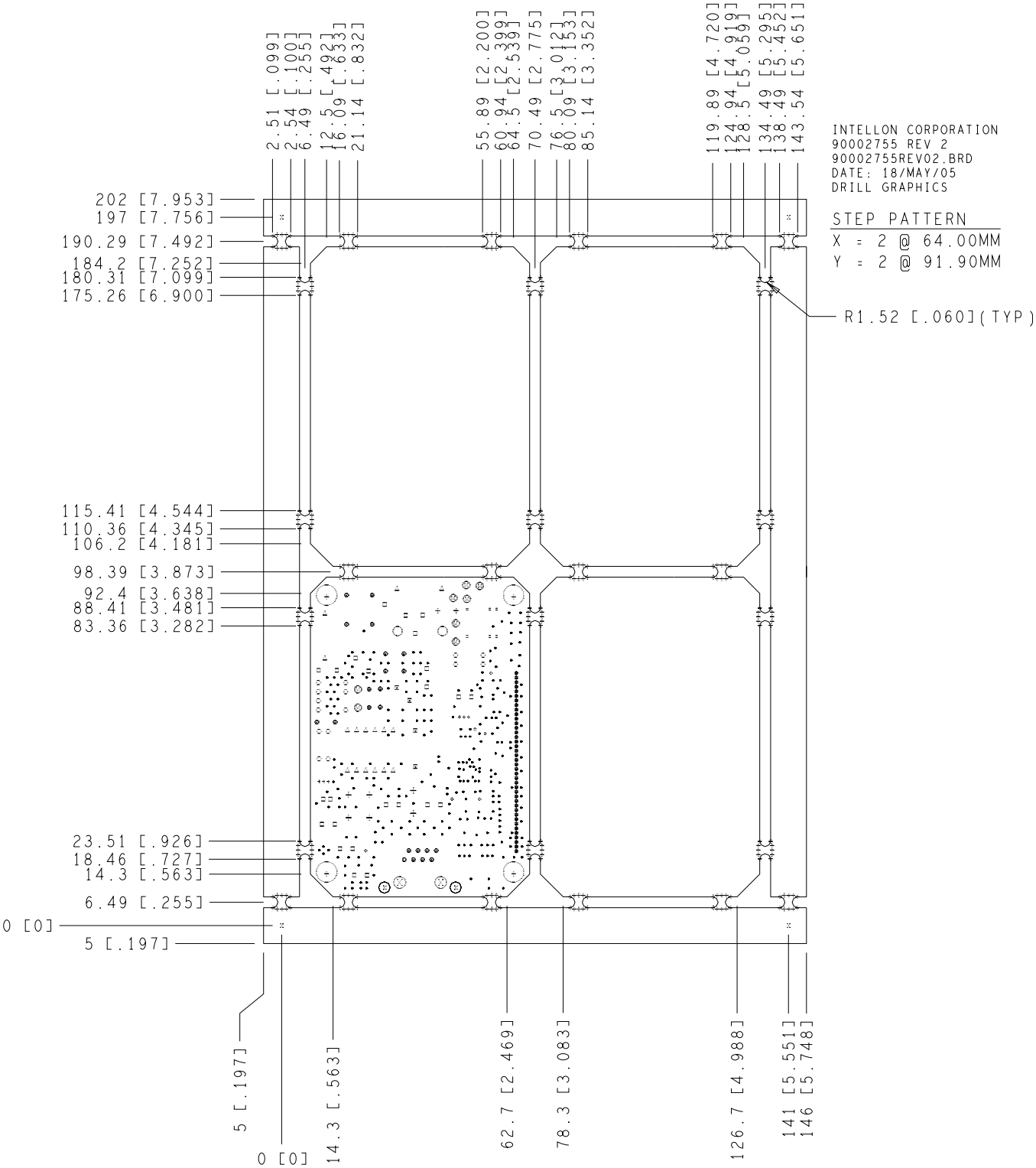
4 Layer Board Stack-up



DWG NO:	80002755
SHEET 2 OF 3	

REVISIONS	
REV	DESCRIPTION
⇒	SEE SHEET 1 FOR REVISION

OUTLINE DRAWING



INTELLON CORPORATION
 90002755 REV 2
 90002755REV02.BRD
 DATE: 18/MAY/05
 DRILL GRAPHICS

DWG	80002755
NO:	
SHEET 3 OF 3	