A26Y10001-DS-01
DH10P 1.0 BETA Specification Sheet

Design of Systems on Silicon
June 10, 2005

REVISION TABLE						
VERSION	DATE			AUTHOR	REVISED BY	APPROVED BY
1.0	June	10	2005	José Luis González		Francisco Andrés

Revision History

REVISION HISTORY					
REVISION	DATE			AUTHOR	LOG
1.0	June	10	2005	José Luis González	Created

DSS9010/DSS7700
PLC MODEM

ØH10P 1.0 BETA
SPECIFICATION SHEET

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1 Product Description

The DH10P reference design is optimized to enable high-speed video and data communications between different devices over the existing domestic power cables. With no configuration, the wall plug provides 100BT Ethernet connectivity and supports transmission speeds in excess of 200 Mbps. The DH10P incorporates DS2 200 Mbps powerline communications technology: the world's highest speed, most fully featured home networking technology, and the only option for transmitting high-quality digital video with full home coverage. Unlike wireless solutions, DS2 PLC networking is not attenuated by walls, and runs on electrical wiring which is present in all homes.

Advanced features such as quality of service management, multicast and network isolation make this the ideal choice for deployment in video on demand or triple play services to connect IP set–top boxes and ADSL residential gateways. Plug and Play autoconfiguration provides consumers with a trouble-free option to network digital devices anywhere in the home without the need for more cabling and gives operators the opportunity provide customers with home-wide services for triple play, video on demand and voice over IP with no need for truck roll.

The DH10P reference design has been developed to minimize cost as well as reduce the format and component count to an absolute minimum. The result is a very low profile design with a minimal bill of materials and advanced manufacturability features such as the Built-In Self Test (BIST). DS2 reference designs provide everything required moving quickly into production of PLC adapters.

1.1 Feature Summary

Highest data rate with bullet-proof reliability

- Dense OFDM for 200 Mbps adaptive PLC networking.
- Powerful error correction system for maximum robustness
- Optimized support for multicast and broadcast traffic

Integrated, low-cost solution

- Low-cost 2-chip solution
- Small 125 mm x 67 mm x 40 mm enclosure

Maximum security

- Mixed DES/3DES encryption guarantees total data security
- 802.1Q VLAN provide powerful tools for isolating traffic

Multiple chip support

- DSS9001 200 Mbps audio/data modem IC with repetition
- DSS9010 200 Mbps data PLC modem IC

Unprecedented flexibility

- Flexible frequency configuration (from 2 to 34 MHz)
- 10 MHz, 20 MHz, and 30 MHz transmission modes
- Flexible MAC for BPL Access and In-Home AV networking

Maximum extensibility

- Flexible API and software development tools
- Remote software upgrade and SNMP support

QoS support

- Up to 8-level priority queues, with programmable priority classification engine (depending on modem IC)
- Programmable bandwidth and latency allocation for advanced QoS provisioning

Standards compliant

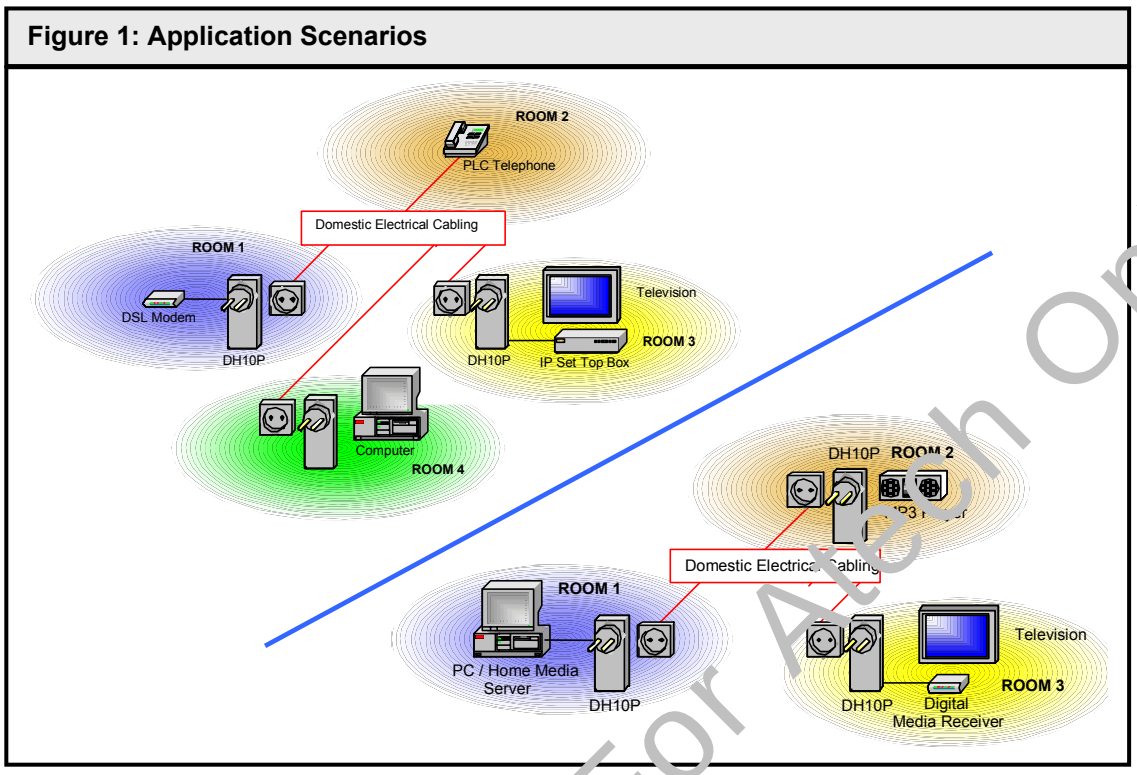
- Support for access/in-home coexistence
- Programmable notching adapts to evolving EMC rules

1.2 Ordering Information

To be defined.

1.3 General Product Information

Figure 1: Application Scenarios



1.4 Included in the RD-DH10P Reference Design

- Gerber Layout Files
- Help Desk Support
- Schematic Files
- Bills of Materials
- Pick and Place File

1.5 Applications

- **Triple Play over DSL** extension– Connect set-top boxes to the DSL modem with no need for cabling
- **Second Receiver for CATV/Satellite** - Watch two different channels in different rooms
- **Networked PVR Players** – Watch multimedia anywhere in the home
- **PC Networking** – Instantly convert a PC into a home media server
- **SOHO Routers** – Better coverage than wireless
- **HDTV Televisions** – Receive content from a remote media server
- **WiFi Extenders** – Overcome the range limitation of wireless

1.6 Application Programming Interface

To facilitate the development of custom applications for the microprocessor embedded in the DS2 digital modem IC, DS2 provides a powerful API. This gives developers the ability to extend and adapt the powerful high-level features provided, such as addition

of applications using the TCP/IP stack, customization of the QoS and networking capabilities.

1.7 Development Environment

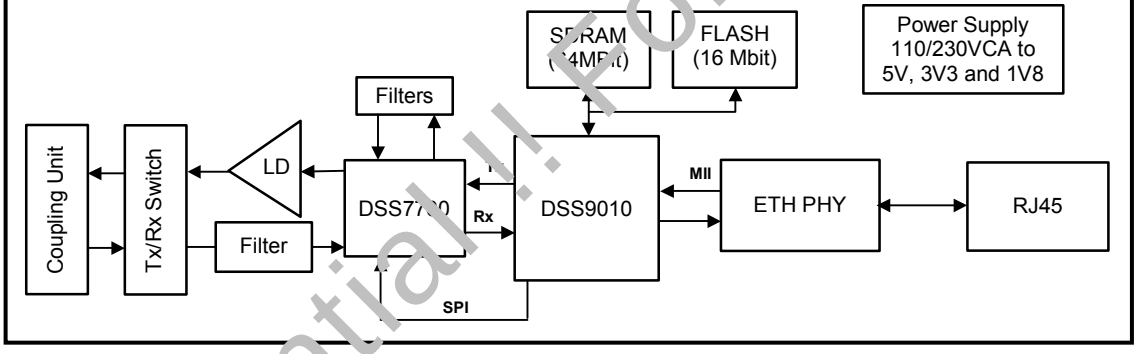
DS2 has created a sophisticated software development environment allowing custom applications to be developed, verified, and added to the extensive features offered by the DS2 digital modem IC device. The development environment is based on industry standard tools for fast and efficient application development.

2 Introduction

The DH10P is a DSS9010-based in-home modem. Its main objective is to extend access to all sockets in the home, covering some of the in-home PLC data market.

The DH10P in-home modem provides a link between the powerline network and a Fast Ethernet 10/100M port.

Figure 2: DSS9010 DH10E Modem Block Diagram



3 Digital Front End

The modem is divided into three blocks: Digital Front End (DFE), Analog Front End (AFE) and Power Supply (PS). The digital front end can be divided into several parts. These parts are:

- DSS9010
- Memory devices (16 megabits of FLASH and 64 megabits of SDRAM)
- Clock circuitry and crystals
- Realtek's RTL8201CL Single Port 10/100M Fast Ethernet Phyceiver
- LEDs and connectors
- Reset and supervisory circuit

3.1 DSS9010

The DSS9010 stands at the core of the in-home modem, at location UD1. It is in charge of controlling all data traffic on the board. It can deliver data rates in excess of 200 Mbps through the powerline port. It is specially designed to operate as a Customer Premises Equipment (CPE) modem or as a home networking device. The DSS9010 forwarding table has room for 16 MAC addresses, making it ideal for developing very low-cost products for the in-home market. The DSS9010 features an industrial standard Media Independent Interface (MII).

3.1.1 DSS9010 Interfaces

3.1.1.1 SPI Interface

An industry standard SPI bus is used by the DSS9010 to interface with several SPI compatible devices. Via the SPI bus, the DSS9010 interfaces with memory devices, analog IC's, etc. The DSS9010 SPI interface supports all four operational modes described in the SPI specification. SPI clock frequencies for each individual SPI compatible device might differ. For this reason, the SPI_CLOCK signal might not necessarily be continuous.

Table 1: SPI Interface Signals			
SIGNAL NAME	**TYPE**	**#**	**DESCRIPTION**
SPI _CLOCK	Output	1	SPI clock. All control and data signals are synchronous to this signal. Frequency is programmable up to 40 MHz.
SPI_OUT	Output	1	SPI serial data out.
SPI_IN	Input	1	SPI serial data in.
SPI_NCS(3:0)	Output	4	Chip select signals for SPI devices.

NOTE: *SPI_NCS(3) is used to select the DSS7700 analog chip.*

3.1.1.2 UART Interface

The DSS9010's UART block is a limited implementation of the 8250 device. The DSS9010 only provides the Tx and Rx lines of the RS-232 standard. A XON-XOFF protocol is needed to communicate between the DSS9010 and a third device. The maximum baud speed of the UART is 9600 bauds.

Table 2: UART Interface Signals			
SIGNAL NAME	**TYPE**	**#**	**DESCRIPTION**
TXD_UART	Output	1	Serial port data out.
RXD_UART	Input	1	Serial port data in.

3.1.1.3 GPIO Interface

The DSS9010 provides nine general-purpose input/output pads. Each of these pads can be configured as input or output. Every input can be used as an IRQ source for the

internal microprocessor. These lines are provided to support customer applications running on the DSS9010.

Besides the functionality assigned to the GPIO signals, these pins also provide access to a CPU JTAG debug port. These signals are multiplexed in such a manner that:

Table 3: GPIO Signals Multiplexing

GPIO	FUNCTION	JTAG
GPIO (0)	-	TCK
GPIO (1)	-	TMS
GPIO (2)	PLC L/A LED	BUSY
GPIO (3)	-	TDI
GPIO (4)	-	TDO
GPIO (5)	HW RESET (NOT YET IN FW)	-
GPIO (6)	-	
GPIO (7)	-	-
GPIO (8)	ETH L/A LED	-

3.2 Memory Devices

There are several memory devices in the DSS9010 DH10P modem. A FLASH memory is used to store boot and firmware code. SST's SST39VF1681 in a TSOP-48 package provides 16 megabits of non-volatile memory, located at UD4.

Besides the FLASH memory, 64 megabits of SDRAM are used as system memory. This SDRAM device operates at clock rates of 160 MHz. The SDRAM used for system memory is Samsung's K4S641632H-TC60 in a TSOP-54 package at location UD3.

3.3 Clock Circuitry and Crystals

CMAC's 80MHZ CPPS-73I-A oscillator of 80MHz and ±25ppm is used at location UD8 as the main system clock, and also as the clock for the internal AD/DA converters inside the DSS9010.

Realtek's RTL8201CL needs a 25 MHz clock signal, which is generated using a 25 MHz crystal at location XD2.

3.4 DH10P External Interfaces

The DSS9010 DH10P modem offers two external interfaces. These interfaces are:

- *Powerline*: This port connects directly to the AC mains. A line coupler protects the modem from the high voltage of the mains and allows through the high frequency data signals. The transmission path converts the data to analog levels, as well as performs the filtering and amplification of the signal before

sending it to the powerline. The reception path amplifies and filters the signal before the analog to digital conversion and the digital demodulation blocks.

- *10/100BaseTx*: The modem offers one Fast Ethernet 10/100 Mbps full duplex interface (half duplex mode not supported) at connector JD2 (RJ45 connector). This interface is implemented with Realtek's RTL8201CL physical layer device at location UD2.

  The RTL8201CL is a single-port phyceiver with an MII/SNI (Serial Network Interface). It integrates 10Base-T and 100Base-TX functions and some extra power management features into a 48-pin single chip, which is used in 10/100 Fast Ethernet applications.

3.5 Power Supply Consumption

There are three main voltages that are used in the DSS9010 DH10P modem: 5 V, 3.3 V and 1.85 V. The 3.3 and 1.85 voltages are filtered to feed the analog front end (3V3_A, 1V8_A). The estimated typical power consumption is shown in Table 4.

Table 4: Typical Power Consumption

OUTPUT	DFE CURRENT (mA)	AFE CURRENT (mA)	TOTAL CURRENT (mA)	POWER (W)
5V	-	200	**200**	1
3V3	170	180	**350**	1.16
1V85	900	4	**904**	1.67
Total Power (W)	-	-	-	**3.82**

3.6 LEDs and Connectors

Three LEDs have been added to the modem to indicate functional status, as well as correct power supply operations. These LEDs are described in the same order as they appear on the front panel of the modem:

Table 5: LED Signals

LED	ON/FLASHING	OPERATION
DL1	PLC link and activity detected	Active low with GPIO (2)
DL3	ETH link and activity detected	Active low with GPIO (8)
DL2	PLC power on	3V3 presence

There are three connectors on the board:

- *External Signal/Power:* Since the DH10P modem has an internal coupling unit and power supply, the modem has an internal power socket connected to signals PLC1 and PLC2. The modem should be connected directly to the AC mains.

- *Ethernet:* The DH10P modem connects to a customer's host PC through an Ethernet port. A pulse jack RJ45 connector with internal magnetics and two LEDs is located at JD2. The two LEDs, green and yellow, are active and blink depending on the status:
  - *Green LED:* Active when the port is linked.
  - *Yellow LED:* Active when the port is linked in 100Base-TX and blinking when transmitting or receiving data.

- *JTAG:* This connector for debugging purposes can be mounted on the bottom side of the board and has the necessary signals for serial communication with the DSS9010 using an external JTAG box. It is stuffed on JD10. Pins 4 and 10 are the SERIAL_RX and SERIAL_TX of the serial interface. It is necessary to add an external transceiver (e.g. MAX232 included in the JTAG box) to adjust the levels of these signals. Table 6 shows the assignment of each pin.

Table 6: JTAG Connector

PIN	NAME	TYPE	FUNCTION
1	+5V	Power	5 Volts
2	CTRL_FLASH	Input	Remote three-state control of the FLASH
3	RESET	Input	External reset
4	SERIAL_RXD	Input	Serial reception
5	TDI	Input	JTAG data input
6	TMS	Input	JTAG control output
7	BUSY	Output	JTAG control input
8	TCK	Input	JTAG clock input
9	GROUND	Power	Ground
10	SERIAL_TXD	Output	Serial transmission
11	TDO	Output	JTAG data output
12	GROUND	Power	Ground

The user should be careful not to insert a connector upside down, since this may cause permanent damage to the user's equipment, as well as the direct connection with a PC serial port without the use of an external transceiver.

3.7 Reset and Supervisory Circuit

There is a single power supply supervisory circuit on the board at location UD9 composed of Maxim's MAX6384XS29D3-T, which supervises 3V3. Whenever 3V3 falls below the factory-set reset thresholds (2.93 V in this case), the reset output asserts and remains asserted for a minimum reset timeout period after 3V3 rises above the reset threshold (140 ms for D3 option) – ±2.5% reset threshold accuracy over temperature (-40°C to +125°C).

4 Analog Front End

4.1 Main Characteristics

- Analog Front End (AFE) based on DS2's DSS7700 PLC analog chip
- Maximum PSD transmitted (30 MHz signal bandwidth): -58 dBm/Hz
- Programmable transmission gain: 25 dB & 13 dB
- Programmable reception gain: 30dB down to -12dB, in 6dB steps
- Maximum signal frequency: 30 MHz
- Coupling unit integrated on the board
- Power supply integrated on the board
- Analog-to-Digital Converter integrated in the DSS9010
- Digital-to-Analog Converter integrated in the DSS9010

4.2 Block Diagram

The AFE is based on the DSS7700 chip. It also includes the line driver, passive filters and the Rx switch.

The DSS7700 incorporates several amplifiers. In transmission, there is a Programmable Gain Amplifier (PGA) before the line driver whose gains can be changed to inject different power levels on the line. In reception there are two amplifiers, the Low Noise Amplifier (LNA) and the PGA for conditioning the received signal to the ADC (Analog-to-Digital Converter) dynamic range.

The PGAs are controlled from the DSS9010 AGC logic algorithm, through the SPI port.

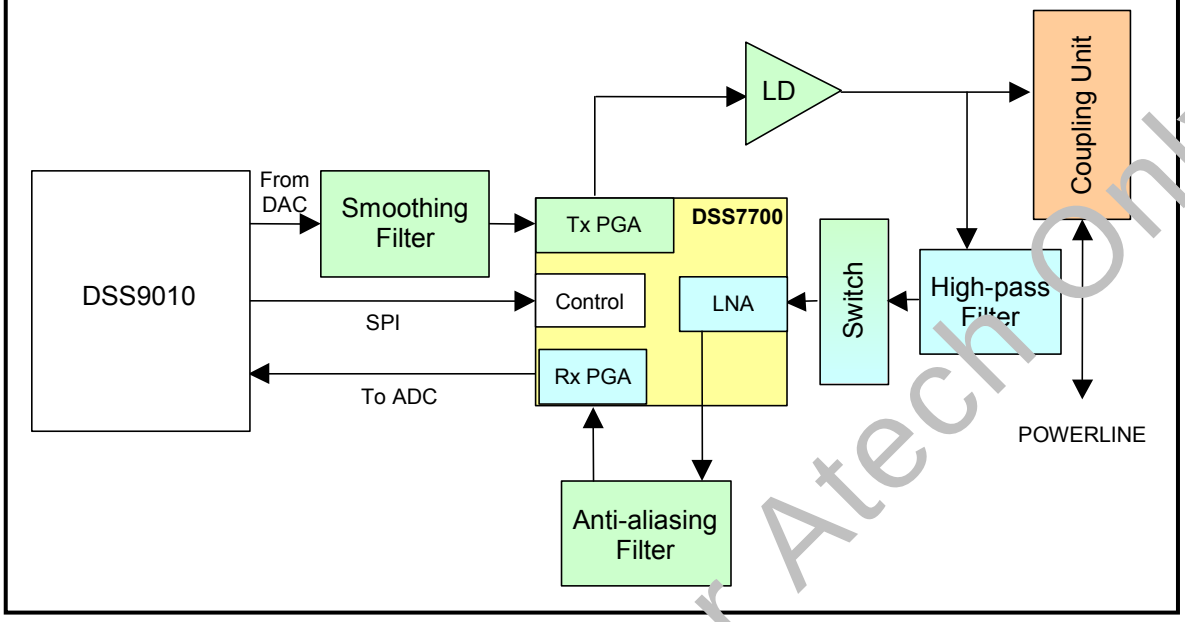
The passive filters are RLC filters designed for shaping the signal in transmission and for rejecting interference frequency bands in reception.

The Rx switch has been designed with bipolar transistors in series with the signal path.

Several debug test and validation features have been implemented in the PCB.

The block diagram is shown in figure 3.

Figure 3: DSS7700-based Analog Front End



The SPI signals from the DSS9010 and the AFE's control signals (reception and transmission gains, etc.) are generated by the firmware and they are the same signals as those found in the DU100.

4.3 Description of the AFE

4.3.1 Transmission Path

The output signal from the Digital-to-Analog Converter (DAC) is filtered by the smoothing filter, and then amplified by the transmission Programmable Gain Amplifier (Tx PGA) from the DSS7700, then continues to the line driver. The signal is then applied to the powerline through the coupling unit.

4.3.2 Reception Path

The reception signal is filtered by the external high-pass filter, enters the reception switch and it is amplified by the Low Noise Amplifier (LNA) from the DSS7700. After that it is filtered by the antialiasing filter and goes to the reception Programmable Gain Amplifier (Rx PGA) from the DSS7700. Then, it passes to the Analog-to-Digital Converter (ADC).

4.3.3 Control

The control of the gains of the different DSS7700 amplifiers and the selection of the Tx and Rx modes are implemented inside the chip, which is controlled by the digital chip via the SPI.

4.4 Coupling Unit

A X1/Y1 capacitor and a signal transformer are used as the coupling unit to the powerline. They also isolate the modem from the powerline voltage.

5 Power Supply

5.1 Specification

The power supply specification is shown in Table 7:

Table 7: Power Supply Specification

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
INPUT						
Voltage (Nominal)	V_{IN}	100		240	VAC	
Frequency (Nominal)	F_{LINE}	50		60	Hz	
OUTPUTS						
Output Voltage 1	V_{OUT1}	3	3.3	3.6	V	For PSD (See Note[1])
Output Ripple Voltage 1	$V_{RIPPLE1}$			200	mV_{PP}	
Output Current 1	I_{OUT1}	0.10	0.35	0.60	A	
Output Voltage 2	V_{OUT2}	1.75	1.85	1.95	V	For PSD (See Note[1])
Output Ripple Voltage 2	$V_{RIPPLE2}$			120	mV_{PP}	
Output Current 2	I_{OUT2}	0.70	0.90	1.10	A	
Output Voltage 3	V_{OUT3}	4.75	5.00	5.25	V	For PSD (See Note[1])
Output Ripple Voltage 3	$V_{RIPPLE3}$			175	mV_{PP}	
Output Current 3	I_{OUT3}	0.15	0.2	0.22	A	
TOTAL OUTPUT POWER						
Typical Output Power	P_{OUT}		3.82		W	
Maximum Output Power	$P_{OUT-MAX}$			5.115	W	
Efficiency	η	65			%	@Full Load 70 ^{O}C

NOTE[1]: *Differential input noise at mains (PSD) –144 dBm/Hz to –150 dBm/Hz from 4 MHz to 34 MHz.*

6 EMC & Safety

DS2 is working to meet with the essential requirements stated in the EMC (89/336/EEC) and Low Voltage (73/23/EEC) European Directives in its DH10P design.

To comply with the requirements of the EMC Directive, DS2 is working to fit its design to pass the corresponding tests stated in the EN 55022 (Emissions), EN 55024 (Immunity), EN 61000-3-2 (Harmonics) and EN 61000-3-3 (Flicker).

To comply with the requirements of the Low Voltage Directive, DS2 is working to fit its design to pass the corresponding tests stated in the EN 60950-1:2001 (IEC 60950-1:2001) standard.

Fulfilling with the above-mentioned standards, the DH10P design will be able to meet with the EMC and Safety requirements for EU CE marking.

7 Environmental Performance

The specifications for DH10P wall plug format are the following:

- Thermal range of 0-40ºC
- Up to 6.6W dissipated in a plastic box
- IP20 protection

8 Mechanical Specifications

8.1 PCBs

The DH10P modem uses two Printed Circuit Assemblies (SB10P and PS10P).

The SB10P board is a 6-layers printed circuit board. Its dimensions are 88 mm x 55 mm (3.464" x 2.165"), and has been manufactured using FR-4 dielectrics. Its thickness between dielectrics is 1.354 mm (53.31 mil).

Its stack-up is the following:

- Layer 1: External Signal layer
- Layer 2: Ground Plane
- Layer 3: Power Plane and Internal Signal layer
- Layer 4: Power Plane
- Layer 5: Ground Plane
- Layer 6: External Signal layer

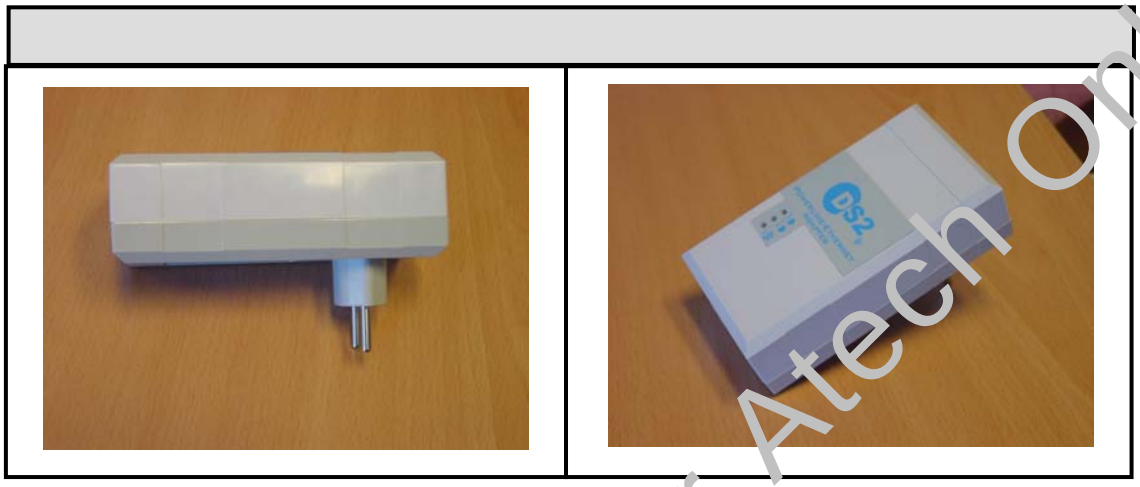
Both external layers are used to mount components.

The PS10P board is a 2-layers printed circuit board. Its dimensions are 88 mm x 55 mm (3.464" x 2.165"), and has been manufactured using one FR-4 dielectric. Its thickness between dielectrics is 1.6 mm (63 mils).

Only the top layer is used to mount components.

8.2 External View

The three status LEDs (previously described) are located on the front panel of the modem and on the bottom side of the enclosure there is a RJ45 Fast 10/100M Ethernet port.



8.3 Plastic Box

The following figures illustrate different points of view of the modem's plastic box.

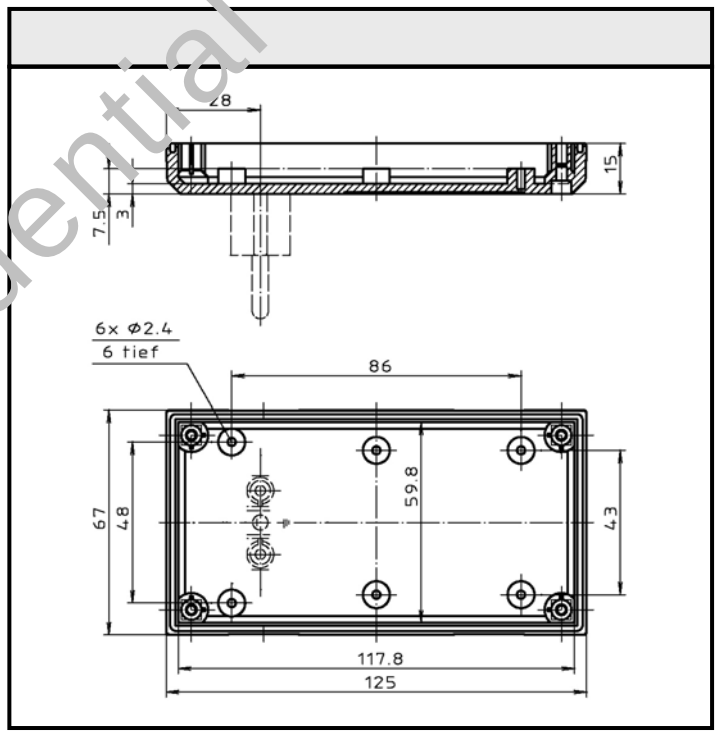


Figure 6: Model of Plastic Lid