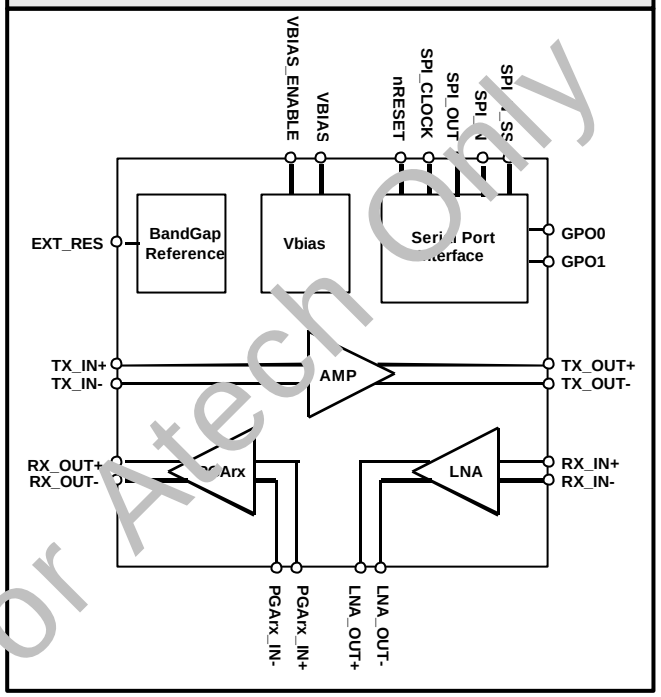
The DSS7700 is a high-speed, programmable, high-performance analog IC for Powerline Communications (PLC) services. It is one of the basic building blocks for a multi-service, broadband, access and local area network over the existing power distribution cables. It can be used for a wide range of market segments, including residential and small business segments, low voltage and medium voltage backbone infrastructures and fiber optic networks.

The DSS7700 is part of DS2's PLC solution chipset and, together with the corresponding external filters and line driver, constitutes a complete Analog Front End (AFE).

It contains a programmable pre-driver (AMP) for the transmission path, and a programmable Low Noise Amplifier (LNA) and a Programmable Gain Amplifier (PGA) for the reception path.

**Figure 1: DSS7700 Block Diagram**




## 1 Feature Summary

- Used for access (Optical gateway, MV/LV gateway, HE, Home Gateway, CPE) and LAN services
- Very low noise and distortion in whole transmission and reception paths
- Power down control for each block of the transmission and reception paths
- Programmable transmission and reception gains
- Programmable Low Noise Amplifier
- Fully differential
- Integrated control logic, SPI interface
- 5V single supply
- 48-pin QFN Package
- Industrial temperature range (-40ºC to 85ºC)

## 2 Ordering Information

| Part Number | Order Code | Package Type | Temperature Range |
|---|---|---|---|
| DSS7700 | **TBD** | QFN 48 | Industrial (-40ºC to 85 ºC) |

Confidential !! For Atech Only

## 3 AFE Modem Application Block Diagram

Figure 2 represents a complete Analog Front End (AFE) for PLC services using the DSS7700.

**Figure 2: AFE Modem Block Diagram**

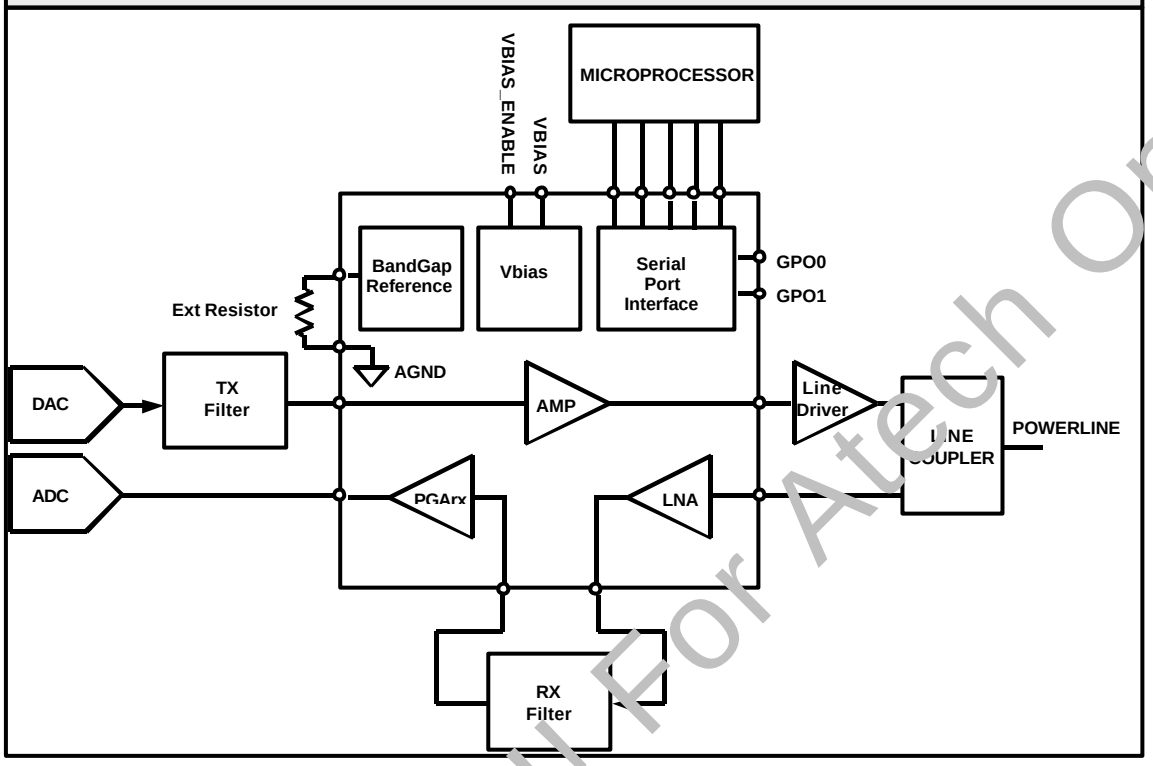
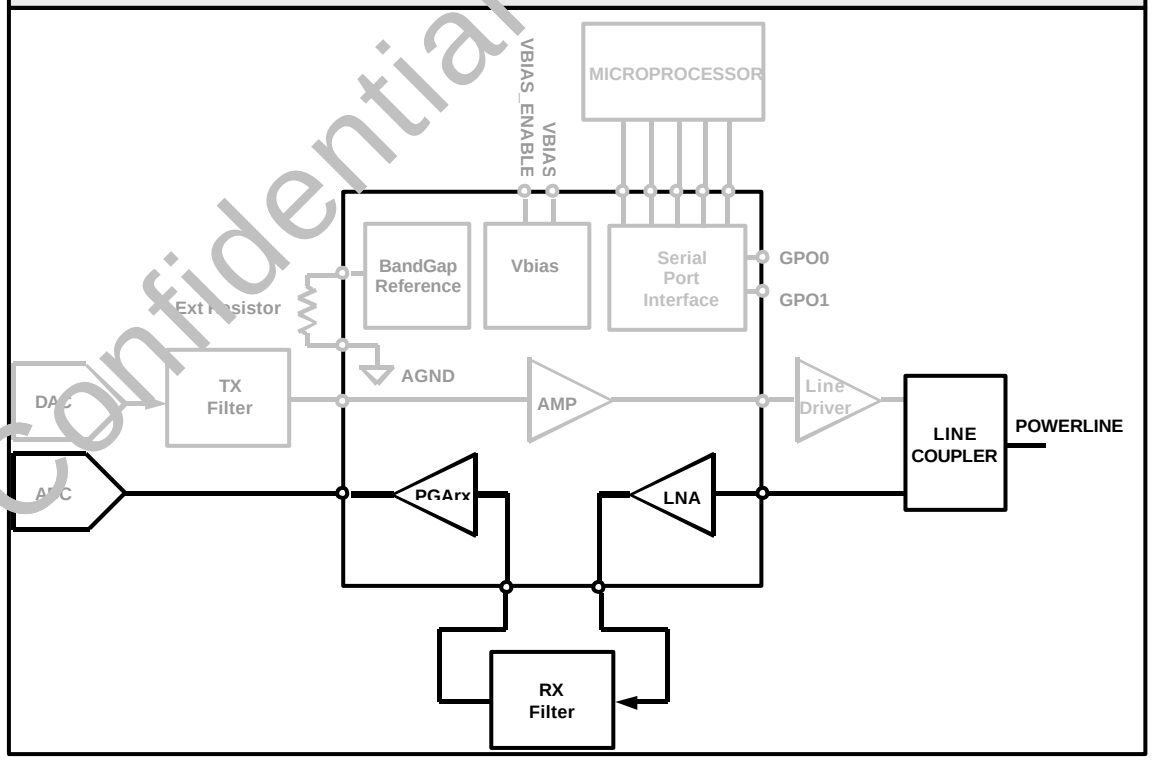
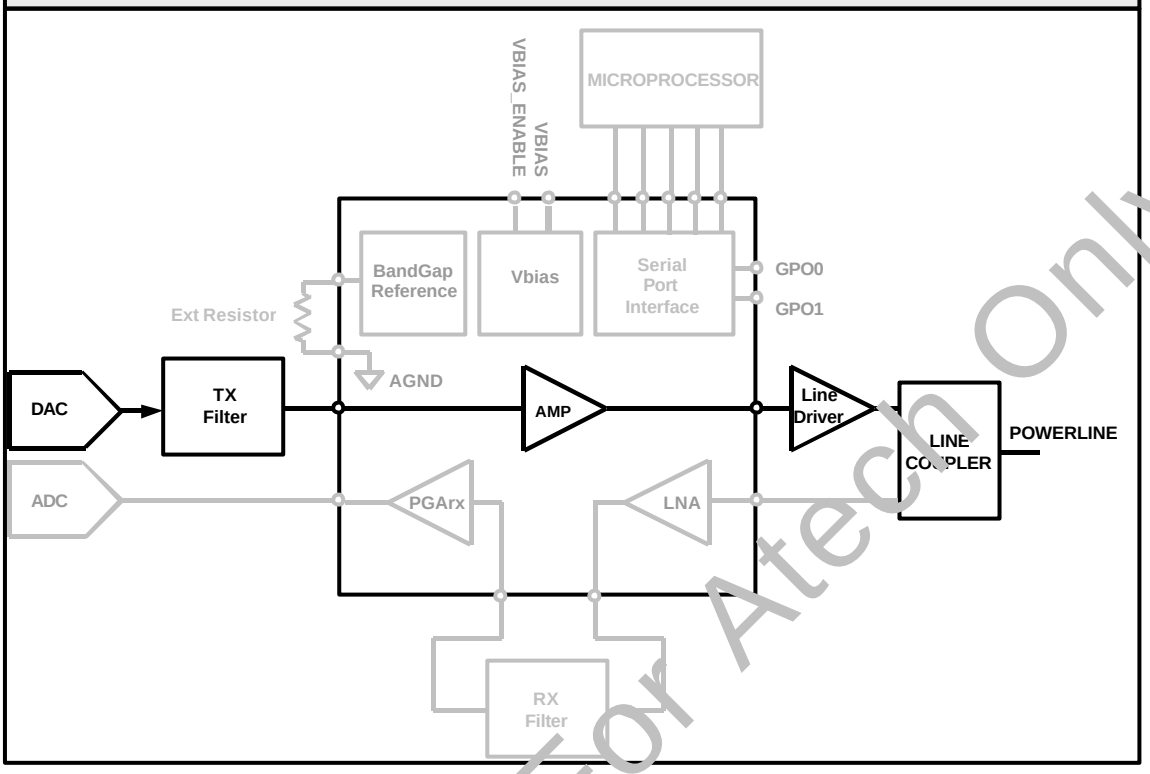



**Figure 3: AFE Modem Receive Path**




Confidential !! For Atech Only

**Figure 4: AFE Modem Transmit Path**




## 4 Pinout

| Pin Number | Mnemonic | Type | Description |
|---|---|---|---|
| 7, 8, 11, 12, 13, 19, 23, 24, 42, 46, 47 | $AV_{DD}$ | S | Analog supply voltage, 5V. These pins should be decoupled using a 100nF capacitor between each $AV_{DD}$ pin and AGND. |
| 3, 4, 14, 15, 16, 20, 25, 26, 43, 44, 45, 48 | AGND | S | Analog ground. Ground reference pins for the analog circuitry. |
| 1,2 | TX_OUT+, TX_OUT- | O | AMP differential outputs.<br>(Differential outputs for transmission channel). |
| 5,6 | TX_IN+, TX_IN- | I | AMP differential inputs.<br>(Differential inputs for transmission channel). |
| 9, 10 | RX_OUT-, RX_OUT+ | O | PGArx differential outputs.<br>(Differential outputs for reception channel). |
| 17,18 | PGArx_IN+, PGArx_IN- | I | PGArx differential inputs. |
| 21,22 | LNA_OUT-, LNA_OUT+ | O | LNA differential outputs. |
| 27, 28 | RX_IN+, RX_IN- | I | LNA differential inputs.<br>(Differential inputs for reception channel). |
| 41 | EXT_RES | O | 1K2 bandgap reference external resistor. |

Confidential !! For Atech Only

| Pin Number | Mnemonic | Type | Description |
|---|---|---|---|
| 40 | EXT_RES_GND | S | Bandgap reference external resistor ground. |
| 38 | VBIAS_ENABLE | I | Power down control signal for internal common mode reference, logic input[1] with internal pull up resistor. A high level on this pin (or by leaving it unconnected) allows the reference to operate normally, whereas a low input level causes the reference circuitry to enter in the power down mode (external reference must be provided). |
| 39 | VBIAS | S | $AV_{DD}/2$, common mode reference. |
| 31 | nRESET | I | Digital input[1], control logic asynchronous reset signal. A low level on this input resets the control logic circuitry and registers to their default state. |
| 35 | SPI_OUT | O | Digital output[2], serial data output. Data is shifted out through this pin on every high to low clock transition during write operations. |
| 37 | SPI_N_SS | I | Digital input[1], slave enable. |
| 32 | SPI_IN | I | Digital input[1], serial data input. Data is shifted in through this pin on every low to high clock transition during read operations. |
| 34 | SPI_CLOCK | I | Digital input[1] control logic serial clock signal. |
| 36 | DGND | S | Digital ground. Ground reference pins for the digital circuitry. |
| 33 | $DV_{DD}$ | S | Digital supply voltage, 5V. This pin should be decoupled using a 100nF capacitor between each $AV_{DD}$ pin and AGND. |
| 30 | GPO0 | O | General purpose digital output 0[2] |
| 29 | GPO1 | O | General purpose digital output 1[2] |

**NOTES:**

[1] TTL & 3.3V LVTTL compatible inputs. See also Section 6.2.

[2] CMOS compatible outputs. See also Section 6.2.

## 5 Circuit Specifications*

### 5.1 Environmental Specifications

| Parameter | Symbol | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| External Temperature | $T_A$ | -40 | 25 | 85 | ºC | |
| Lead Temperature | | | 240 | | ºC | Sn-Pb Eutectic Assembly (10-30 seconds) |
| | | | 250 | | ºC | Pb-Free Assembly (20-40 seconds) |

Confidential !! For Atech Only

## 5.2 Electrical Specifications

| Parameter | Symbol | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| Analog Supply Voltage | $AV_{DD}$ | 4.75 | 5 | 5.25 | V | |
| Digital Supply Voltage | $DV_{DD}$ | 4.75 | 5 | 5.25 | V | |
| Power Dissipation Tx Mode | $P_{WRTX}$ | | 270 | | mW | |
| Power Dissipation Rx Mode | $P_{WRRX}$ | | 700 | | mW | |

## 5.3 AMP Transmission Amplifier Specifications

| Parameter | Symbol | Min | Typ | Max | Units | Note |
|---|---|---|---|---|---|---|
| Differential Input Signal | $V_{ID}$ | | | 1 | Vpp | |
| Minimum Gain | | | 0 | | dB | |
| Maximum Gain | | | 12 | | dB | |
| Output Voltage Range | $V_{OUT}$ | | | 4 | Vpp | 12dB gain |
| Input Signal Frequency | | | | 40 | MHz | |
| MTPR[2] | | | 69 | | dBc | |
| Input Referred Noise[1] | | | -148 | | dBm/Hz | 12dB gain |
| Differential Input Resistance | $R_{IN}$ | | 2.1 | | KΩ | |
| Differential Input Capacitance | $C_{IN}$ | | 1.7 | | pF | 12dB gain |
| Power Consumption | | | 270 | | mW | |

**NOTES:**

[1] 50Ω referred.

[2] DS2 multi-carrier signal.

***** Values expected by design; Not guaranteed by test.

## 5.4 PGAmx Specifications

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential Output Signal | $V_{OD}$ | | | 2 | Vpp | |
| Minimum Gain | | | 6 | | dB | |
| Maximum Gain | | | 30 | | dB | |

Confidential !! For Atech Only

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Gain Step | | | 6 | | dB | 6, 12, 18, 24, 30dB |
| Input Signal Frequency | | | | 40 | MHz | |
| MTPR[2] | | | 57 | | dBc | |
| Input Referred Noise[1] | | | -147<br>-152 | | dBm/Hz | 6dB gain<br>30dB gain |
| Differential Input Resistance | $R_{IN}$ | | 23.4 | | KΩ | |
| Differential Input Capacitance | $C_{IN}$ | | 1.4 | | pF | |
| Power Consumption | | | 300 | | mW | |

**NOTES:**

[1] 50Ω referred.

[2] DS2 multi-carrier signal.

## 5.5 LNA Specifications

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Differential Output Signal | $V_{OD}$ | | | 2 | Vpp | |
| Minimum Gain | | | -12 | | dB | |
| Maximum Gain | | | 18 | | dB | |
| Gain Step | | | 6 | | dB | -12,-6,0, 6,12,18dB |
| Input Signal Frequency | | | | 40 | MHz | |
| MTPR[2] | | | 57 | | dBc | |
| Input Referred Noise[1] | | | -135<br>-152 | | dBm/Hz | -12dB gain<br>18dB gain |
| Differential Input Resistance | $R_{IN}$ | | 24 | | KΩ | |
| Differential Input Capacitance | $C_{IN}$ | | 5 | | pF | |
| Power Consumption | | | 400 | | mW | |

**NOTES:**

[1] 50Ω referred.

[2] DS2 multi-carrier signal.

Confidential !! For Atech Only

## 6 Serial Peripheral (SPI)

The DSS7700 serial port interface is composed of the following control signals:

- **SPI_IN:** Received data input
- **SPI_OUT:** Transmitted data output
- **SPI_CLOCK:** Serial clock input
- **SPI_N_SS:** Slave select input (active-low signal)
- **NRESET:** Reset input (active-low signal)
- **GPO1/GPO0:** General purpose outputs

### 6.1 Description

The serial interface has an active-low enable (SPI_N_SS) to bracket the data with data clocked in MSB first on the rising edge of SPI_CLOCK. Data is stored in the storage latch on the rising edge of SPI_N_SS. The serial interface controls the state of all DSS7700 blocks (see Section 0).

Every transmission to the SPI slave is a write/read operation, except for the first access which shifts a fixed value that can be read by the firmware to detect the current SPI slave version. Therefore the first read/write operation does not have any effect on the DSS7700 internal register. Note also that it is necessary to send the whole 16 control bit register on every read/write operation to properly update the DSS7700 storage latch.

A SPI master device can read the value shifted out by the DSS7700 SPI, which corresponds to the one stored in its storage latch. The master SPI clock control bits must be properly set (CPHA = 1, CPOL = 1) according to the standard SPI protocol.

### 6.2 DC Electrical Characteristics

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| Vil | Low level input voltage | - | 0.8 | V |
| Vih | High level input voltage | 2.0 | - | V |
| Iil | Low level input current | - | -1.0 | uA |
| Iih | High level input current | - | 1.0 | uA |
| Vol | Low level output voltage | - | 0.4 | V |
| Voh | High level output voltage | 4.0 | - | V |
| Iol | Low level output current | - | 4.0 | mA |
| Ioh | High level output current | - | -4.0 | mA |

Confidential !! For Atech Only

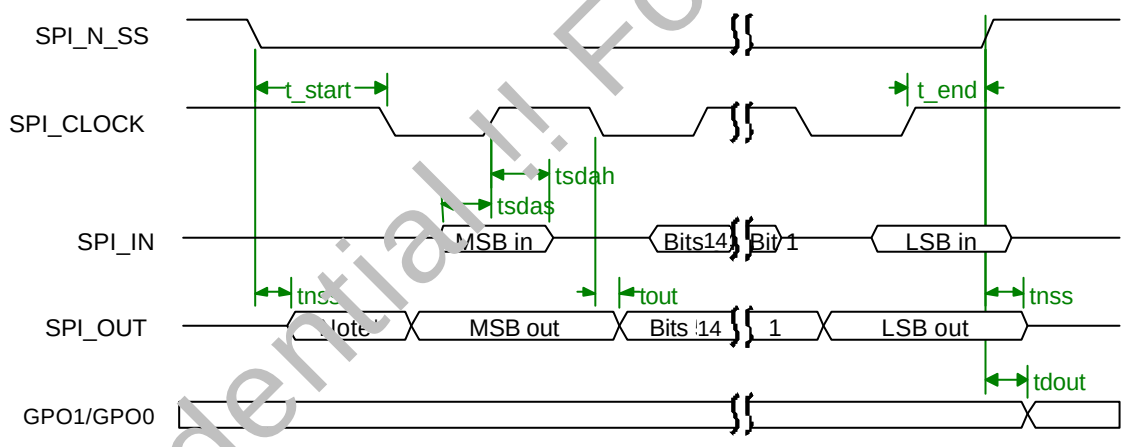
### 6.3 AC Electrical Characteristics

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Max frequency | SPI_CLOCK max. frequency | - | - | 40 | MHz |
| t_start | Start clock after SPI_N_SS low | 15 | - | - | ns |
| t_end | End clock before SPI_N_SS high | 15 | - | - | ns |
| tsdas | Input SPI_IN setup vs. SPI_CLOCK | 1 | - | - | ns |
| tsdah | Input SPI_IN hold vs. SPI_CLOCK | 0 | - | - | ns |
| tout[1] | SPI_OUT delay from SPI_CLOCK low | 0 | - | 7.1 | ns |
| tnss | Data enable/disable time | - | - | 20 | ns |
| tdout[1] | GPO1/GPO0 delay from SPI_N_SS high | 0 | | 26.6 | ns |

**NOTE:**

[1] Assuming a 10pF output load.

**Figure 5: AC Electrical Characteristics**




NOTE: LSB of the character previously transmitted

## 7 Chip State Control Bits

### 7.1 PGArx control bits

| Table 1: PGArx Control Bits Assignment | | | |
|---|---|---|---|
| **Bit** | 13 | 12 | 11 |
| **Name** | A3 | A2 | A1 |

Confidential !! For Atech Only

| Table 2: PGArx Control Bits Description | | |
|---|---|---|
| **Name** | **Default** | **Description** |
| A3 | 0 | Gain selection.<br>See Table 3 for valid combinations |
| A2 | 0 | |
| A1 | 0 | |

| Table 3: PGArx Control Bits Valid Combinations | | | |
|---|---|---|---|
| **Gain** | **A3** | **A2** | **A1** |
| Power down mode | 0 | 0 | 0 |
| 6dB | 1 | 0 | 0 |
| 12dB | 0 | 1 | 0 |
| 18dB | 1 | 1 | 0 |
| 24dB | 0 | 0 | 1 |
| 30dB | 1 | 0 | 1 |

## 7.2 Transmission Amplifier Control Bits

| Table 4: Transmission Amplifier Control Bits Assignment | | |
|---|---|---|
| **Bit** | 15 | 14 |
| **Name** | PD_Control | S_Control |

| Table 5: Transmission Amplifier Control Bits Description | | |
|---|---|---|
| **Name** | **Default** | **Description** |
| S_Control | 0 | Gain control bit. See table 6. |
| PD_Control | 0 | Power down mode (active low) |

| Table 6: Transmission Amplifier Control Bits Valid Combinations | | |
|---|---|---|
| **PD_Control** | **S_Control** | **Gain** |
| 0 | 0 | Power down mode |
| 0 | 1 | 0dB |
| 1 | 0 | 12dB |

Confidential!! For Atech Only

### 7.3 LNA Control Bits

| Table 7: LNA Control Bits Assignment | | | |
|---|---|---|---|
| **Bit** | 7 | 6 | 5 |
| **Name** | E3 | E2 | E1 |

| Table 8: LNA Control Bits Description | | |
|---|---|---|
| **Name** | **Default** | **Description** |
| E3 | 0 | Gain selection<br>See table 9 for valid combinations |
| E2 | 0 | |
| E1 | 0 | |

| Table 9: LNA Control Bits Valid Combinations | | | |
|---|---|---|---|
| **Gain** | **E3** | **E2** | **E1** |
| Power down mode | 0 | 0 | 0 |
| -12dB | 1 | 0 | 0 |
| -6dB | 0 | 1 | 0 |
| 0dB | 1 | 1 | 0 |
| 6dB | 0 | 0 | 1 |
| 12dB | 1 | 0 | 1 |
| 18dB | 0 | 1 | 1 |

### 7.4 GPO1 & GPO0 General Purpose Output Signals

| Table 10: GPO1 & GPO0 Control Bits Assignment | | |
|---|---|---|
| **Bit** | 2 | 1 |
| **Name** | GPO1 | GPO0 |

**Table 10: GPO1 & GPO0 control bits assignment**

| Table 11: GPO1 & GPO0 Control Bits Description | | |
|---|---|---|
| **Name** | **Default** | **Description** |
| GPO1 | 0 | General purpose output signal 1 |
| GPO0 | 0 | General purpose output signal 0 |

Confidential !! For Atech Only

### 7.5 Programming Example

In order to illustrate how the DSS7700 can be programmed the following example is presented. Suppose that DSS7700 is to be programmed as follows:

- **Transmission Channel 2(0dB total gain):** AMP (0dB gain)
- **Reception Channel 1 (24dB total gain):** LNA (18dB gain) + PGArx (6dB gain)

The following bit sequence should be issued to the DSS7500:

**Table 12: Bit Sequence Example**

| PD_Control | S_Control | A3 | A2 | A1 | - | E3 | E2 | E1 | - | GPO1 | GPO0 | - |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AMP | | PGArx | | | - | LNA | | | - | GPO1 | GPO0 | - |
| 15 | 14 | 13 | 12 | 11 | 10-8 | 7 | 6 | 5 | 4-3 | 1 | 1 | 0 |
| **0** | **1** | **1** | **0** | **0** | **000** | **0** | **1** | **1** | **00** | **0** | **0** | **0** |

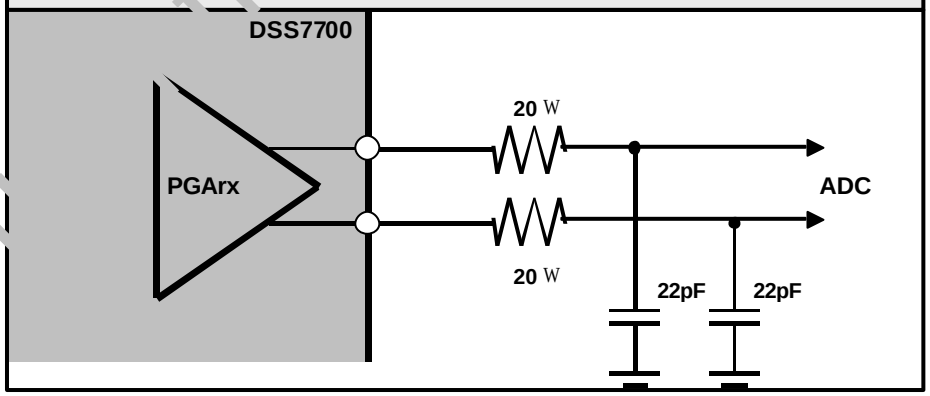
Note that bits in positions 10-8, 4-3 and 0 have no meaning and must be set to 0.

## 8 PGArx Output Capacitance

PGArx has been internally compensated to maximize its performance when loading an ADC with a certain amount of capacitive load. Therefore, in order to ensure PGArx stability, a minimum capacitive load of 22pF between both PGArx outputs and ground is necessary as shown in Figure 6.

In addition, a resistor placed in series with PGArx outputs is recommended for increasing device phase margin when loading large capacitive loads.

**Figure 6: Recommended PGArx Output Capacitance**




Confidential !! For Atech Only

# 9 Biasing considerations

## 9.1 Normal Operation (Internally Biased)

If VBIAS_ENABLE is either connected to AVDD or left open (this input features an internal pull-up resistor) then DSS7700 inputs are internally biased to CMref (AVDD/2). In this case a 100pF ceramic capacitor must be connected between VBIAS and GND to provide a low impedance internal biasing voltage.

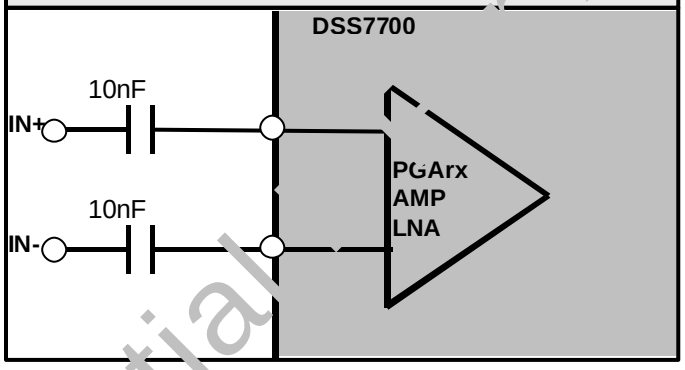
## 9.2 External Biasing

If an external reference is to be used, the VBIAS_ENABLE signal must be set to 0. In this mode VBIAS is the voltage reference input, and must be driven by an external AVDD/2 voltage source. This voltage source should exhibit a low output impedance along the whole input signal bandwidth. It should be able to both sink and source transient currents.

## 9.3 Decoupling of Inputs

In both modes, analog inputs need to be DC decoupled as shown in Figure 7.

**Figure 7: Recommended Decoupling**



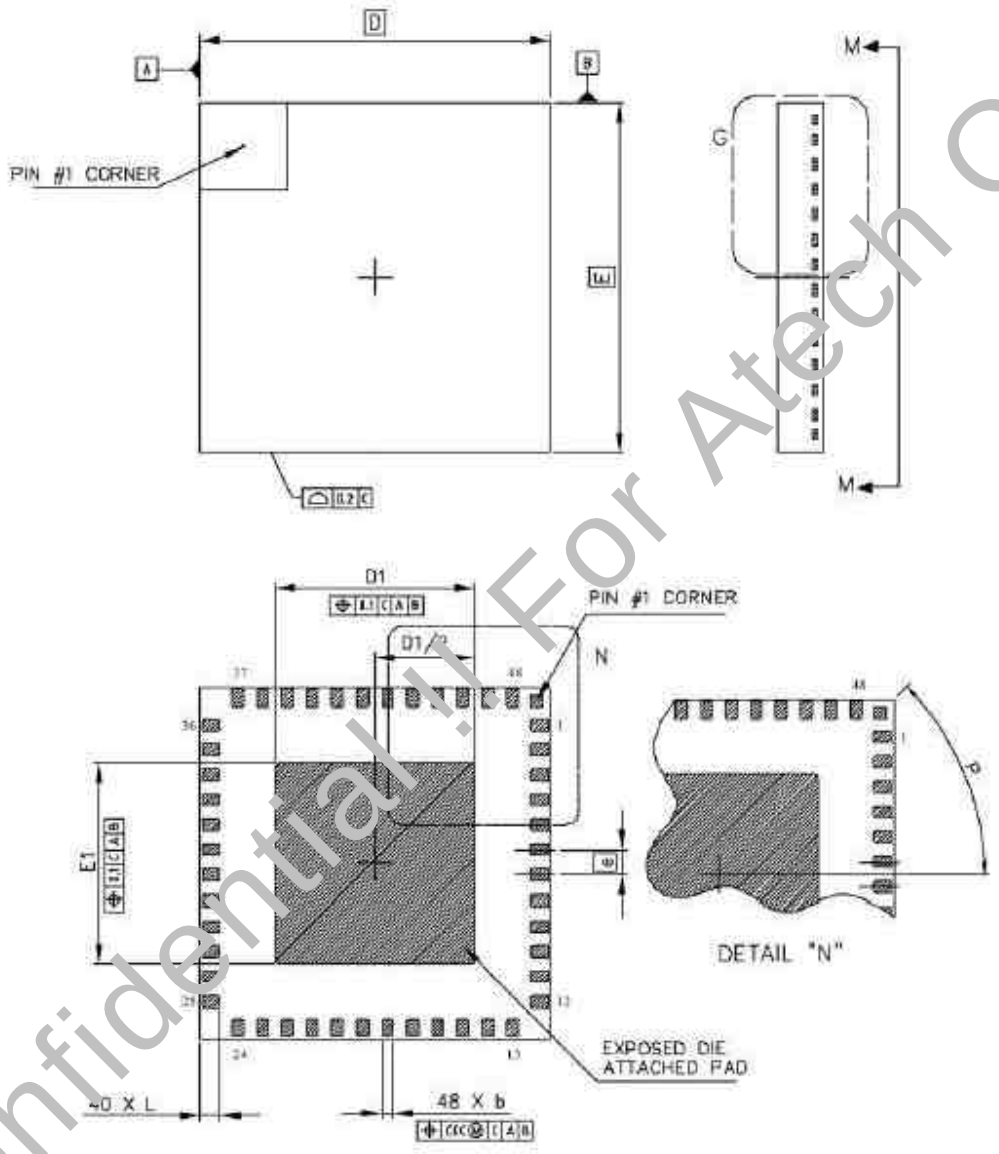

# 10 Exposed Pad Considerations

In order to improve thermal performance, the DSS7700 features an exposed die attached pad. This element is electrically connected to AGND. The PCB should provide adequate heat removal from the IC by connecting the exposed pad to the PCB AGND plane. Precautions must be taken to ensure a proper electrical and thermal path between the exposed pad and the ground plane when designing the PCB.

Confidential - Atech Only

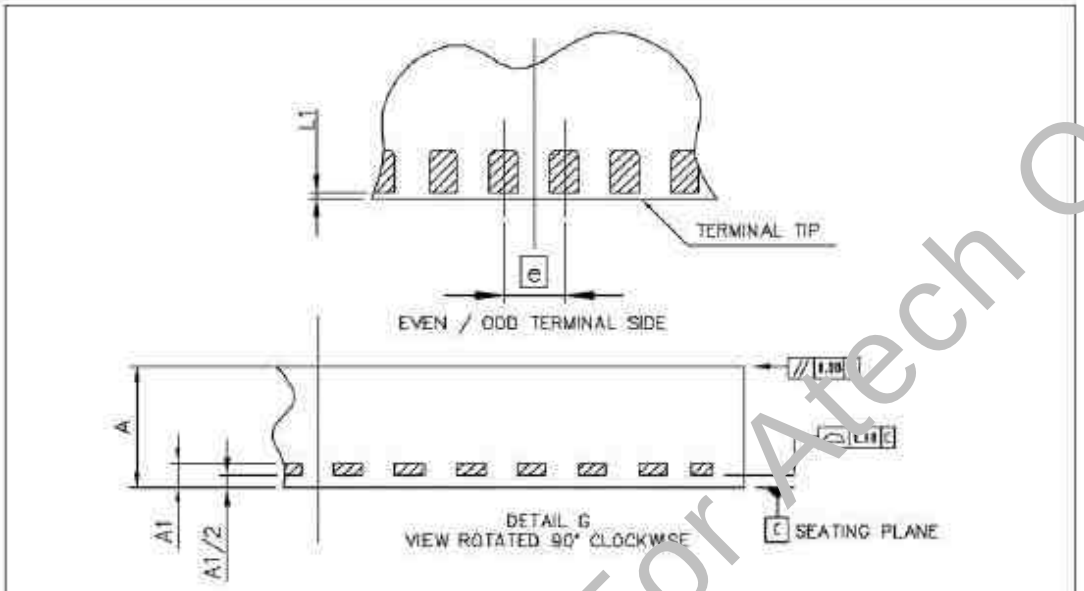
## 11 Package Outline

**Figure 8: Package Outline**




Confidential !! For Atech Only

**Table 12: Package Outline & Dimensions**




| DIM | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.80 | | 1.00 |
| A1 | | 0.203 REF | |
| b | 0.18 | 0.23 | 0.30 |
| D | | 7.00 BSC | |
| E | | 7.00 BSC | |
| D1 | 3.90 | | 4.10 |
| E1 | 3.90 | | 4.10 |
| e | | 0.50 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | | | 0.10 |
| P | | 45° BSC | |
| aaa | | 0.15 | |
| ccc | | 0.10 | |

NOTES

ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

Confidential !! For Atech Only

## Index

**1 Feature Summary ..... 1**

**2 Ordering Information ..... 1**

**3 AFE Modem Application Block Diagram ..... 2**

**4 Pinout ..... 3**

**5 Circuit Specifications* ..... 4**

5.1 Environmental Specifications ..... 4
5.2 Electrical Specifications ..... 5
5.3 AMP Transmission Amplifier Specifications ..... 5
5.4 PGArx Specifications ..... 5
5.5 LNA Specifications ..... 6

**6 Serial Peripheral (SPI) ..... 7**

6.1 Description ..... 7
6.2 DC Electrical Characteristics ..... 7
6.3 AC Electrical Characteristics ..... 8

**7 Chip State Control Bits ..... 8**

7.1 PGArx control bits ..... 8
7.2 Transmission Amplifier Control Bits ..... 9
7.3 LNA Control Bits ..... 10
7.4 GPO1 & GPO0 General Purpose Output Signals ..... 10
7.5 Programming Example ..... 11

**8 PGArx Output Capacitance ..... 11**

**9 Biasing considerations ..... 12**

9.1 Normal Operation (Internally Biased) ..... 12
9.2 External Biasing ..... 12
9.3 Decoupling of Inputs ..... 12

**10 Exposed Pad Considerations ..... 12**

**11 Package Outline ..... 13**

Confidential !! For Atech Only