The DSS9010 is a low-cost integrated circuit, optimized to enable high-speed video and data communications between different devices over the existing domestic power cables. As a member of the DSS90*xx* family, the DSS9010 supports transmission speeds in excess of 200Mbps and additional features like QoS management, multicast and network isolation using 3DES encryption.

The DSS9010 supports multiple Medium Access Control protocols, each one optimized for a different application. Support for slave mode in the DS2 Access MAC ensures that the DSS9010 can be used for low-cost customer premises equipment in PLC access and in-building deployment. Support for an In-Home AV MAC makes the device suitable for deployment in home networking, allowing networks to support multiple classes of service. Each DSS9010 in a network can be programmed to support the class of service for its own type of traffic.

The DSS9010 supports a full set of autoconfiguration features ensuring that end users have an immediate out of the box Plug and Play experience. All aspects of network configuration can be set up automatically such as network domain and passwords, quality of service levels, frequency selection, etc.

Quality of Service (QoS) capabilities are provided with multiple priority levels and strict bandwidth and latency guarantees, allowing network operators to provide any type of service with stringent QoS requirements, like VoIP, TV or Video on Demand.

The DSS90*xx* is the only PLC product family to incorporate remotely programmable notching, ensuring the dynamic adaptability of installed units to comply with current and future global regulatory requirements.

DS2 provides a family of chips designed with the required flexibility and throughput capabilities for home networking applications. The DSS9010 shares the same physical layer characteristics with the DSS90*xx* series of PLC modem devices, allowing seamless integration of access and in-home networks. Advanced OFDM modulation provides the ability to cope with the changing characteristics of the powerline channel using high-density constellations that provide a throughput of more than 200 Mbps.

The DSS9010 can be easily integrated with the DSS7700, which provides a single analog front end perfectly adapted for PLC. The DSS7700 contains very low noise, low distortion amplifiers demanded by dense OFDM applications. Assembled in a 48-pin QFN package, the device runs from a single 5V supply and provides advanced features such as power-down control for each block and a programmable gain amplifier for automatic gain control.

1 Feature Summary

Highest data rate with bulletproof reliability

- Dense OFDM provides adaptive powerline data rates in excess of 200Mbps
- Powerful Error Correction System provides maximum robustness in any powerline environment
- Optimized support for multicast and broadcast traffic

Integrated, low-cost solution

- Low-cost, 2-chip solution when used with DSS7*xxx* family of analog ICs
- Integrated 802.1D Ethernet bridge
- Integrated 10/100 base T interface reduces the cost of interconnection with other network devices
- SPI, GPIO and UART interfaces
- Integrated ADC, DAC and AGC
- Integrated clock generation

Maximum security

- Mixed DES/3DES encryption guarantees total data security
- 802.1Q VLAN provide powerful tools for isolating traffic

Unprecedented flexibility

- Flexible frequency configuration (from 2 to 34MHz)
- 10MHz, 20MHz, and 30MHz transmission modes
- Flexible MAC (point-to-multipoint master-slave, point-to-point master-slave, and peer-to-peer) for in-home and access networks (only slave mode is supported for master-slave MAC)

Maximum extensibility

- Flexible API and software development tools
- Remote software upgrade and SNMP support

QoS support

- Priority marking to ensure correct traffic prioritization
- Programmable bandwidth and latency allocation for advanced QoS provisioning

Standards compliant

- Support for access/in-home coexistence
- Technology compliant with FCC Part 15, EN55022 EMC limits
- Programmable powermask provides compatibility with current and future EMC regulations

2 Ordering Information

Part Number	Order Code	Package Type	Temperature Range
DSS9010	**XXXXXX-XX-X**	HSBGA196	**X**

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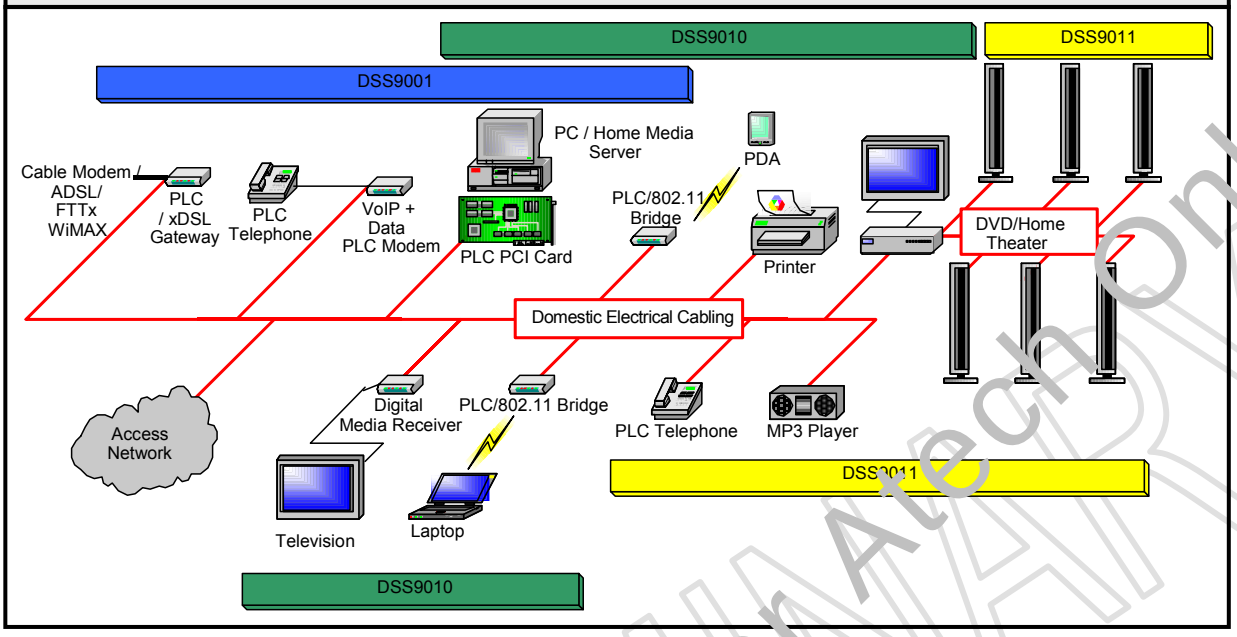
3 General Product Description

Figure 1



3.1 Applications

- **Triple Play over DSL** – Connect set-top boxes to the DSL modem with no need for cabling
- **Second Receiver for CATV/Satellite** - Watch two different channels in different rooms
- **Networked PVR Players** – Watch multimedia anywhere in the home
- **Home Theater** – Distribute audio anywhere in the home
- **PC Motherboards** – Instantly convert a computer into a home media server
- **SOHO Routers** – Better coverage than wireless
- **HDTV Televisions** – Receive content from a remote media server
- **WiFi Extenders** – Overcome the range limitation of wireless

3.2 Application Programming Interface

To facilitate the development of custom applications for the microprocessor embedded in the DSS9010, DS2 provides a powerful API. This gives developers the ability to extend and adapt the powerful high-level features provided, such as addition of applications using the TCP/IP stack, customization of the QoS and networking capabilities.

3.3 Development Environment

DS2 has created a sophisticated software development environment allowing custom applications to be developed, verified, and added to the extensive features offered by the DSS9010 device. The development environment is based on industry standard tools for fast and efficient application development.

3.4 Reference Designs

DS2 has developed a complete set of reference designs for user modems as well as for infrastructure equipment. The designs have been thoroughly validated for EMC and thermal performance, and can provide an advanced foundation for manufacturers seeking to minimize their time to market.

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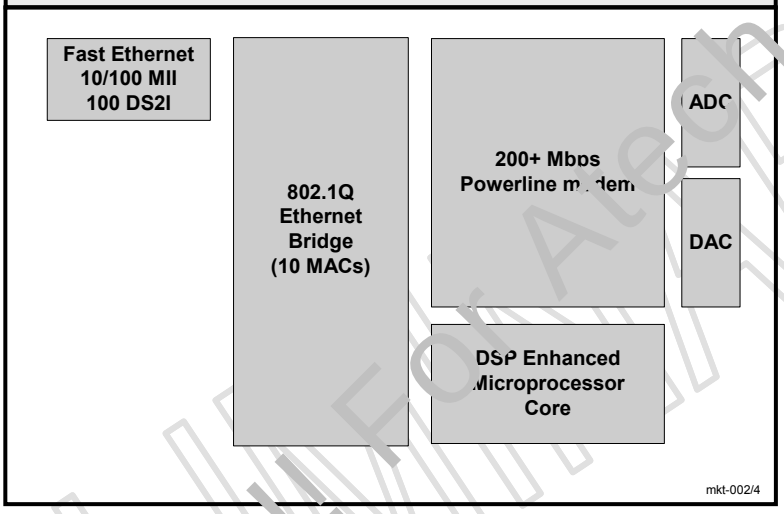
3.5 Evaluation Equipment

DS2 produces and sells limited volumes of evaluation equipment based on the reference designs. This allows customers to rapidly prototype and evaluate networking projects using DS2's PLC technology, and provides a development platform for network and solution prototyping.

4 DSS9010 Block Diagram

The DSS9010 is specially designed to operate as a Customer Premises Equipment (CPE) modem or as a home networking device. The DSS9010 forwarding table has room for 16 MAC addresses, making it ideal for developing very low-cost products for the residential market.

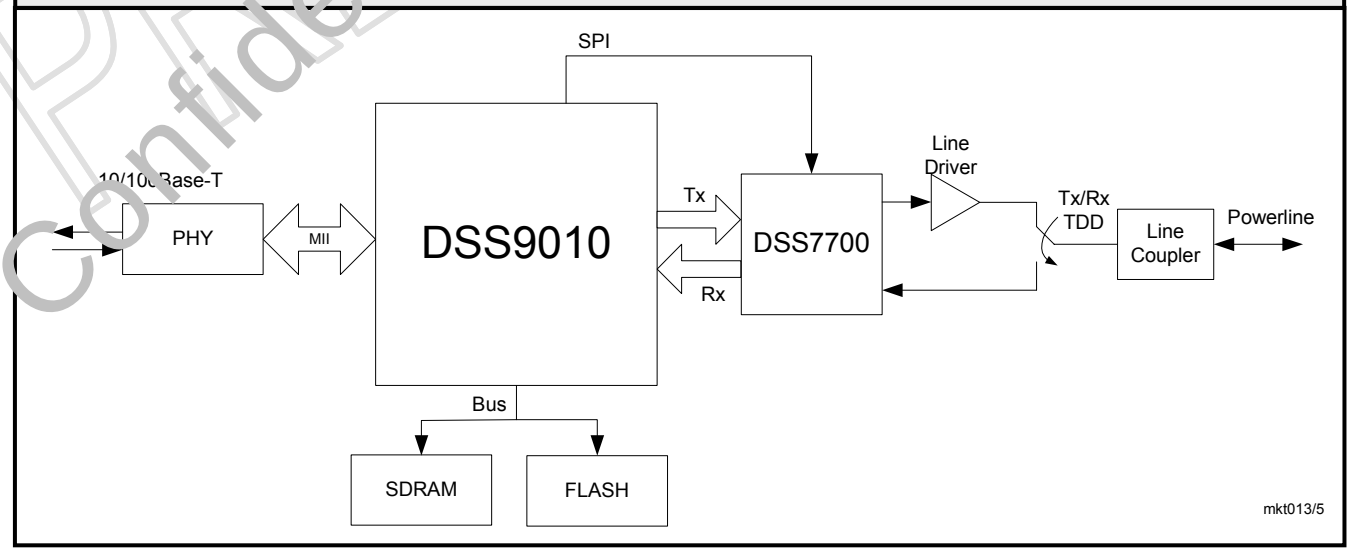
Figure 2: DSS9010 Block Diagram



5 Applications

The DSS9010 is intended to work as a home networking device. Thanks to its Fast Ethernet interface it can be easily connected to any type of computer or appliance. Figure 3 depicts a typical application of the DSS9010 as a PLC to Ethernet bridge.

Figure 3: Block Diagram of a Customer Premises Equipment



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6 DSS9010 Technical Features

As a member of the DSS90*xx* family, the DSS9010 shares many of the common features of the DSS90*xx* series of ICs. For more information about the features of the DSS90*xx* family, please consult the *DSS90xx Family Datasheet*.

7 External Interfaces

Besides the powerline port, the DSS9010 provides three standard external interfaces:

- MII
- SPI
- UART

7.1 MII

The DSS9010 incorporates an industry standard Media Independent Interface (MII). This interface connects an Ethernet MAC to a PHY, and supports data transmission rates of up to 100Mbps.

The DSS9010 can be configured to work in MAC (Medium Access Control) mode. When operating in MAC mode, an external 10/100BaseT PHY should be connected to this interface.

SIGNAL NAME	TYPE	#	DESCRIPTION
RXD(3:0)	Input	4	**Receive data**. These signals are synchronous to RX_CLK.
RX_ER	Input	1	**Receive error**. This pin is asserted when an error is detected on the RXD(3:0) lines.
RX_DV	Input	1	**Receive data valid**. This signal is asserted high when received data is present on the RXD(3:0) lines. This signal is deasserted at the end of the packet and is synchronous to RX_CLK.
RX_CLK	Input	1	**Receive clock**. It provides a continuous clock reference for RX_DV and RXD(3:0). 10BaseT: 2.5MHz. 100BaseTX: 25MHz.
TXD(3:0)	Output	4	**Transmit data**. These signals are synchronous to TX_CLK. The MAC will source TXD(3:0) when TX_EN is asserted.
TX_EN	Output	1	**Transmit enable**. This signal indicates the presence of valid nibble data on TXD(3:0).
TX_CLK	I/O	1	**Transmit clock**. It provides a continuous clock reference for TX_EN and TXD(3:0). 10BaseT: 2.5MHz (I). 100BaseTX: 25MHz (I).
MDC	Output	1	**Management interface clock**.
MDIO	I/O	1	**Management interface input/output**. This pin provides the bi-directional signal used to transfer management information.

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Figure 4: MII Receive

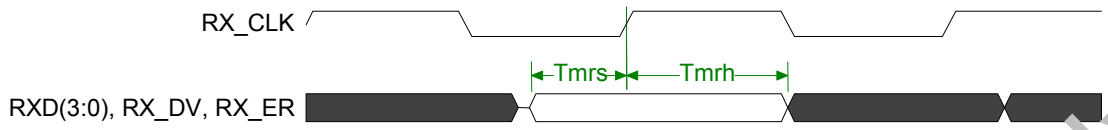
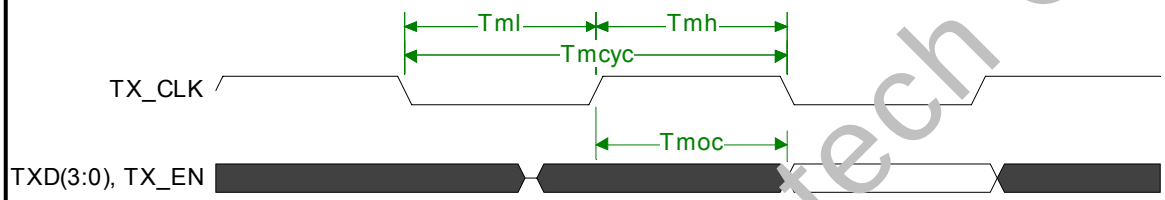


Figure 5: MII Transmit



7.2 SPI

An industry standard SPI bus is used by the DSS9010 to interface with several SPI compatible devices. Via the SPI bus, the DSS9010 interfaces with memory devices, analog ICs, and voice processing codecs/SLICSs. The DSS9010 SPI interface supports all four operational modes described in the SPI specification. SPI clock frequencies for each individual SPI compatible device might differ. For this reason, the SPI_CLOCK signal might not necessarily be continuous.

SIGNAL NAME	TYPE	#	DESCRIPTION
SPI _CLOCK	Output	1	SPI clock. All control and data signals are synchronous to this signal. Frequency is programmable up to 40MHz.
SPI_OUT	Output	1	SPI serial data out.
SPI_IN	Input	1	SPI serial data in.
SPI_NCS (3:0)	Output	4	Chip select signals for SPI devices.

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Figure 6: SPI Write

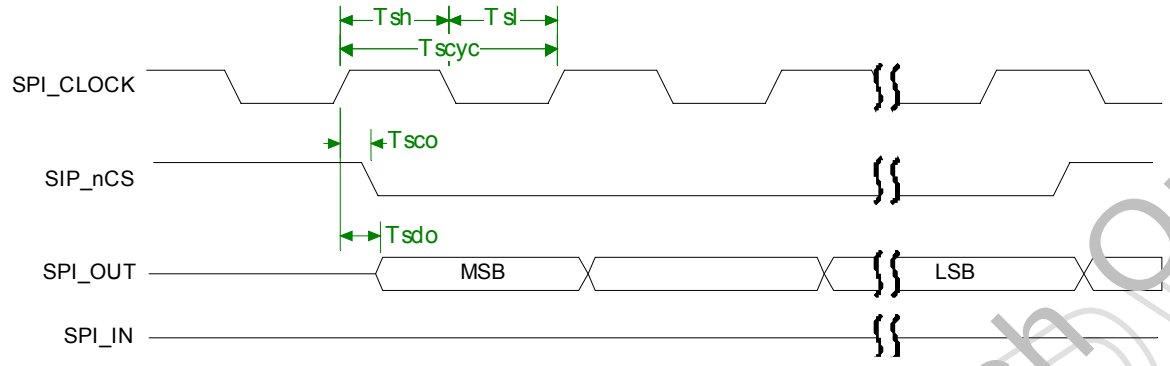

Figure 7: SPI Read

7.3 UART

The DSS9010's UART block is a limited implementation of the 8250 device. The DSS9010 only provides the TX and RX lines of the RS-232 standard. A XON-XOFF protocol is needed to communicate between the DSS9010 and a third device. The maximum baud speed of the UART is 115200 bauds.

SIGNAL NAME	TYPE	#	DESCRIPTION
TXD_UART	Output	1	Serial port data out.
RXD_UART	Input	1	Serial port data in.

8 Coexistence

The DSS9010 has been developed to coexist with future PLC technologies. In access or in-home situations there can be several PLC networks sharing the channel, each of them implemented with technology from different vendors. All of these technologies should coexist with one another and not hinder any communication among them.

Those nodes that want to transmit data in an in-home scenario where other technologies are present must contend for the use of the channel. Coexistence with other technologies has been implemented using a RTS/CTS protocol. A node that contends for the channel sends a SOT signal once it detects that the channel is free (the channel is considered free after detection of an EOT signal, or after a certain time has elapsed since the last SOT was

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detected). This SOT signal is sent after a predetermined time after the channel is detected free, which is based on the eight levels of packet priority. After the SOT signal is sent, the modem starts transmitting data, and sends an EOT signal once the transfer of data is finished. At this point the channel is considered free again.

The coexistence functional block has been implemented inside the DSS9010. However, in order to provide flexibility to the user, these signals have been connected to external pins as well, multiplexed with GPIO(8:0) signals.

SIGNAL NAME	TYPE	#	DESCRIPTION
CLOCK_COEX	Output	1	Coexistence clock.
REQUEST_COEX(2:0)	Output	3	Priority signals. Eight levels of priority are possible.
RESPONSE_COEX(1:0)	Input	2	Result of channel contention.
RCV_SOT_COEX	Output	1	Receive SOT signal.
RCV_EOT_COEX	Output	1	Receive EOT signal.
SEND_EOT_COEX	Input	1	Send EOT signal.

9 Memory Interface

The DSS9010 interfaces with 16-bit wide memory devices with clock rates of 160MHz. A 64-megabit (4 banks x 1M x 16bit) CAS latency-3 synchronous DRAM is used for system memory. A FLASH device with an access speed of 150ns or faster is used for boot and firmware storage purposes. Data and address lines are shared between SDRAM and FLASH devices.

SIGNAL NAME	TYPE	#	DESCRIPTION
SDRAM_CLOCK	Output	1	160MHz clock output for SDRAM devices.
SDRAM_CLK_FB	Input	1	160MHz clock feedback. Connected to SDRAM_CLOCK.
NCS_FLASH	Output	1	FLASH device chip select.
NOE_FLASH	Output	1	FLASH device output enable.
SDRAM_NCS	Output	1	SDRAM device chip select.
NRAS	Output	1	SDRAM row access strobe.
NCAS	Output	1	SDRAM column access strobe.
NWE	Output	1	Memory write enable.
BA(1:0)	Output	2	Bank address: Selects bank to be activated during RAS# activity. Selects bank to be read/written during CAS# activity.
ADDR(11:0)	Output	12	Memory device address.
DQ(15:0)	I/O	16	16 bit data input/output.
DQM	Output	2	Controls SDRAM output buffers in read mode and masks input data to SDRAM in write mode. DQM_H: Masks DQ(15:8). DQM_L: Masks DQ(7:0).

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Figure 8: FLASH Memory Read Access

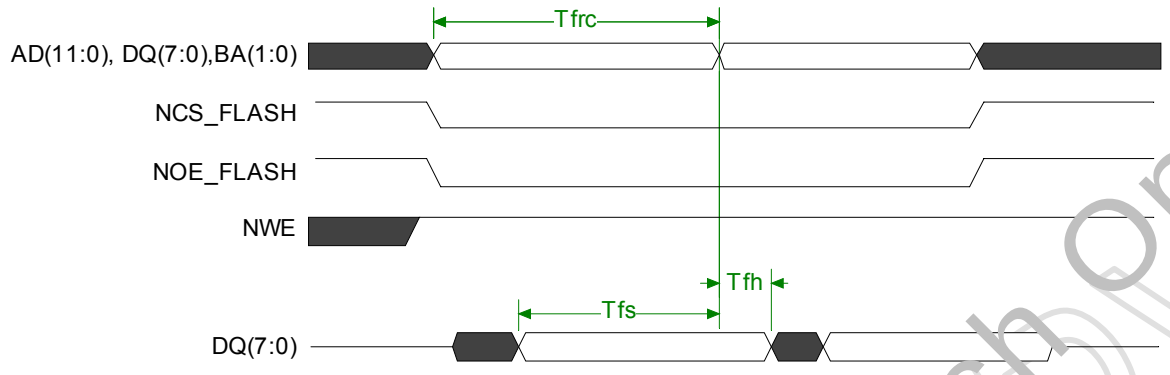

Figure 9: FLASH Memory Write

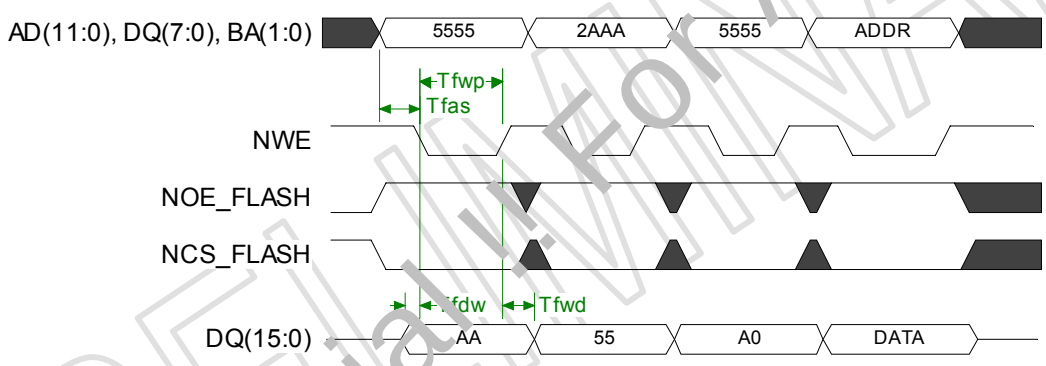

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Figure 10: SDRAM Power-Up Sequence

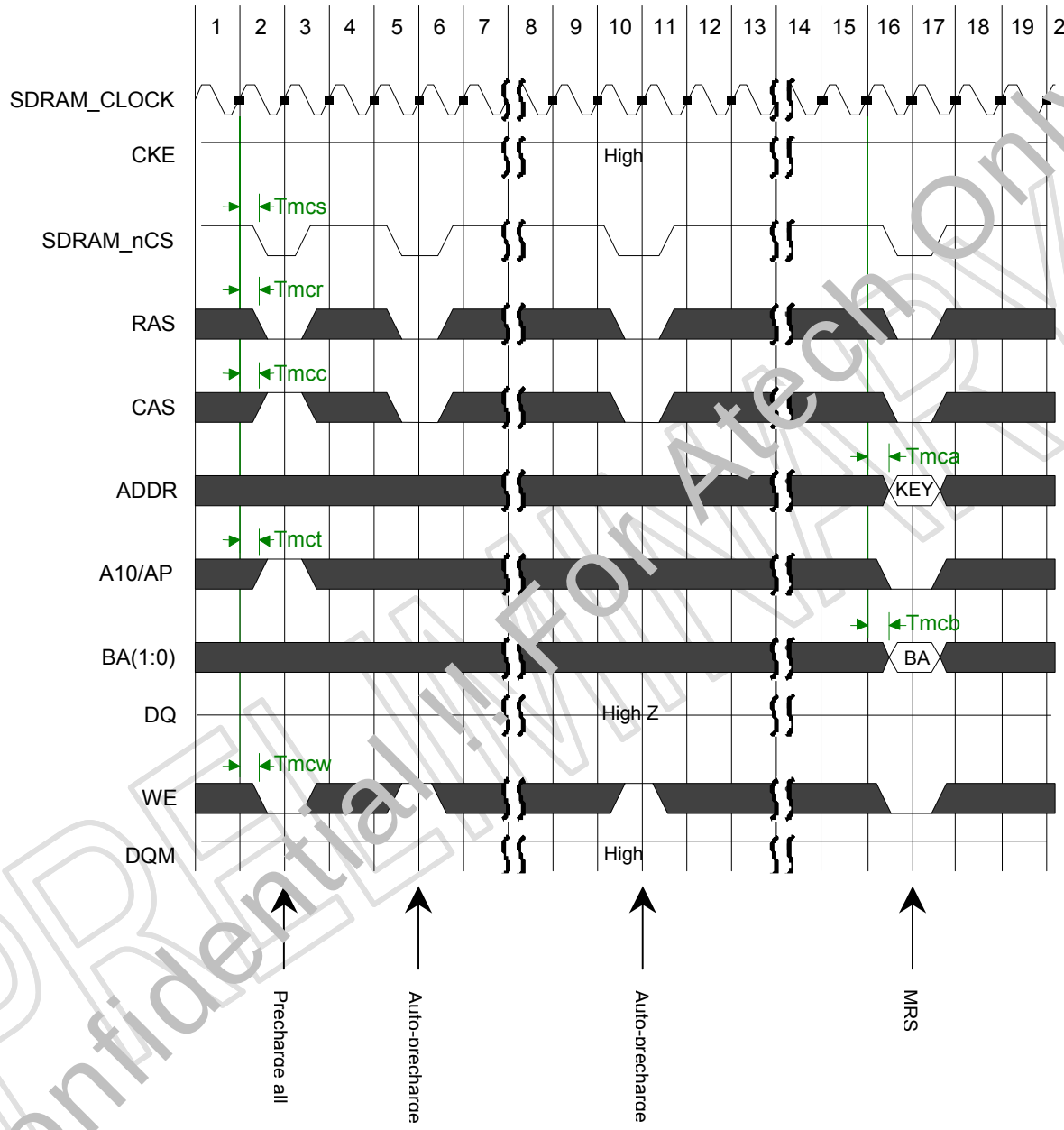

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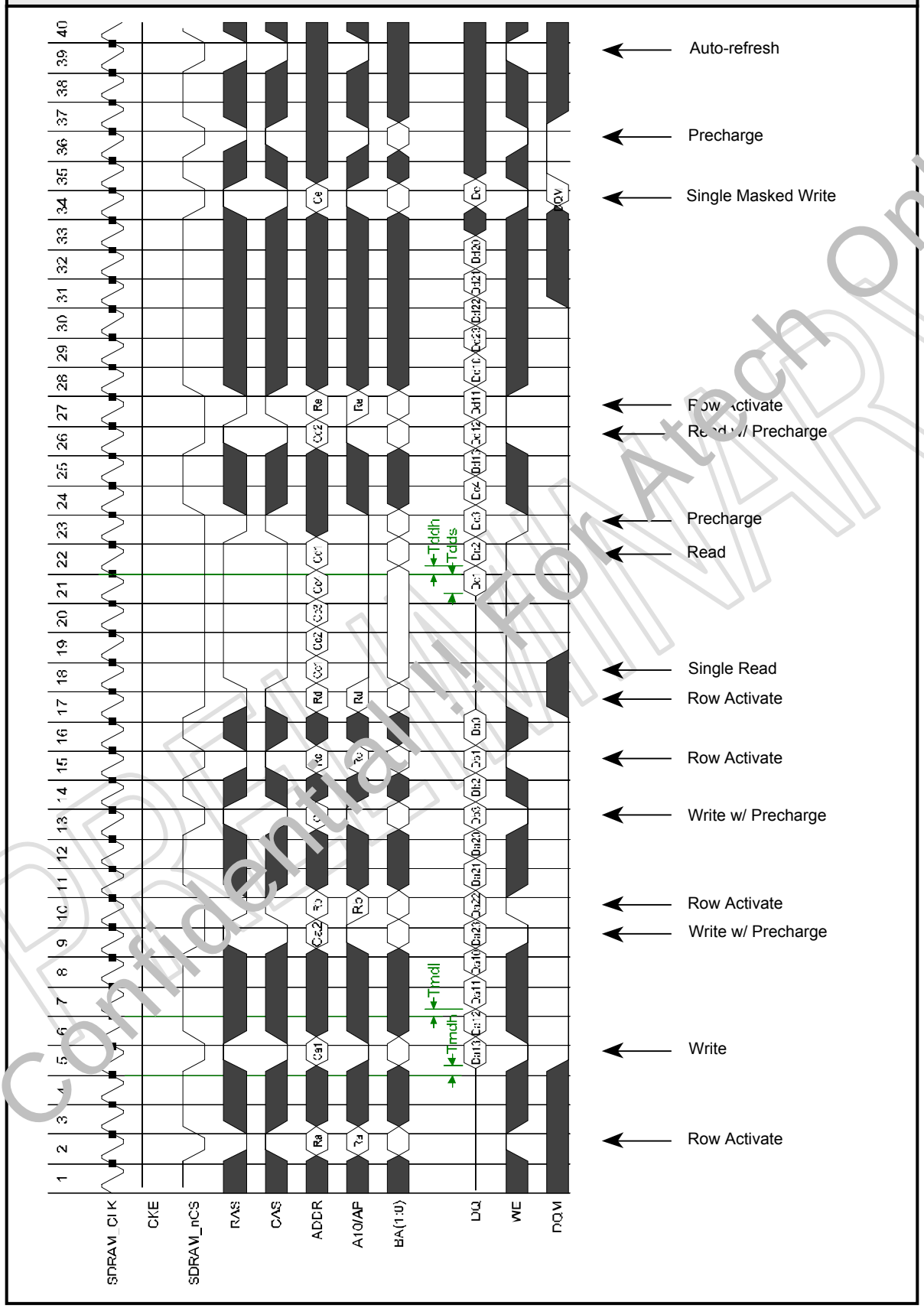
Figure 11: SDRAM Access Sequences



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10 GPIO

The DSS9010 provides nine general-purpose input/output pads. Each of these pads can be configured as input or output. Every input can be used as an IRQ source for the internal microprocessor. These lines are provided to support customer applications running on the DSS9010.

Besides the functionality assigned to the GPIO signals, these pins also provide access to a CPU JTAG debug port. These signals are multiplexed in such a manner that:

GPIO	JTAG
GPIO(0)	TCK
GPIO(1)	TMS
GPIO(2)	BUSY
GPIO(3)	TDI
GPIO(4)	TDO

GPIO	JTAG
GPIO(5)	-
GPIO(6)	-
GPIO(7)	-
GPIO(8)	

11 Electrical Specifications

11.1 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
V_{CORE}	Supply Voltage	-0.3	1.95	V
V_{IO}	I/O Supply Voltage	-0.3	3.6	V
V_{ANL_3V3}	3.3V Analog Supply	-0.3	3.6	V
V_{IN}	DC Input Voltage 3.3V Input Buffer	-0.3	3.9	V
	5V Tolerant Input Buffer	-0.3	6.5	V
T_{STG}	Storage Temperature	-65	150	ºC
T_{SOL}	Soldering Lead Temperature (10 seconds)	--	210	ºC

11.2 DC Electrical Characteristics

SYMBOL	DESCRIPTION	MIN	TYP.	MAX	UNIT
V_{CORE}	Supply Voltage	1.75	1.8	1.85	V
V_{IO}	I/O Supply Voltage	3.25	3.3	3.35	V
V_{ANL_3V3}	3.3V Analog Supply	3.25	3.3	3.35	V
T_A	Temperature Range		--		ºC
V_{IH}	Input High Voltage (LVTTL)	2.0		V_{IO}	V
V_{IL}	Input Low Voltage (LVTTL)	0		0.8	V
V_{OH}	Output High Voltage (LVTTL)	2.4		--	V
V_{OL}	Output Low Voltage (LVTTL)	--		0.4	V

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11.3 AC Electrical Characteristics

SYMBOL	DESCRIPTION	MIN	TYP.	MAX	UNIT
T_{MRS}	MII receive data setup time	10			ns
T_{MRH}	MII receive data hold time	10			ns
T_{MOC}	MII transmit clock to data out	0		25	ns
T_{MCYC}	MII clock cycle time	37.5	40		ns
T_{ML}	MII clock high time	18.75	20		ns
T_{MH}	MII clock low time	18.75	20		ns
T_{SCYC}	SPI clock cycle time	25		6410.2	ns
T_{SL}	SPI clock high time	12.5		3205.1	ns
T_{SH}	SPI clock low time	12.5		3205.1	ns
T_{SCO}	SPI write clock to chip select activate	0			ns
T_{SDO}	SPI write clock to data out	0		45	ns
T_{SCD}	SPI read clock to chip select deactivate	0			ns
T_{SDS}	SPI data setup time	8			ns
T_{SDH}	SPI read data hold time	0			ns
T_{FRC}	FLASH access cycle time	170			ns
T_{FS}	FLASH read cycle set-up time	25			ns
T_{FH}	FLASH read cycle hold time	0			ns
T_{FAS}	FLASH write enable delay	0			ns
T_{FWP}	FLASH write enable pulse time	145			ns
T_{FDW}	FLASH write data WE setup time	0			ns
T_{FWD}	FLASH write data WE hold time	0			ns
T_{DDH}	SDRAM read data hold time	2			ns
T_{DDS}	SDRAM read data setup time	0.75			ns
T_{MCS}	SDRAM clock to chip select	1		4.75	ns
T_{MCR}	SDRAM clock to RAS	1		4.75	ns
T_{MCC}	SDRAM clock to CAS	1		4.75	ns
T_{MCA}	SDRAM clock to valid address	1		4.75	ns
T_{MCT}	SDRAM clock to auto precharge	1		4.75	ns
T_{MCB}	SDRAM clock to BA(1:0)	1		4.75	ns
T_{MCW}	SDRAM clock to write enable	1		4.75	ns
T_{CYC}	SDRAM clock cycle time		6.25		ns
T_{MCD}	SDRAM clock to data out	1		4.75	ns
T_{MDL}	Clock to data output in low-Z time	1			ns
T_{MDH}	Clock to data output in high-Z time			4.75	ns
T_{RC}	RAS cycle time	14			SDRAM_CLK
T_{RCD}	RAS to CAS delay	3			SDRAM_CLK
T_{RAS}	RAS active time	10			SDRAM_CLK
T_{RP}	RAS precharge time	4			SDRAM_CLK
T_{RRD}	RAS to RAS bank active delay	2			SDRAM_CLK
T_{CCD}	CAS to CAS delay	1			SDRAM_CLK
T_{WTL}	Write command to data-in delay	0			SDRAM_CLK

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SYMBOL	DESCRIPTION	MIN	TYP.	MAX	UNIT
T_{DPL}	Data-in to precharge command	2			SDRAM_CLK
T_{DAL}	Data-in to active command	6			SDRAM_CLK
T_{DQZ}	DQM to data-out Hi-Z	2			SDRAM_CLK
T_{DQM}	DQM to data-in mask	0			SDRAM_CLK
T_{MRD}	MRS to new command	2			SDRAM_CLK
T_{REF}	Refresh time			64	SDRAM_CLK

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12 Pin Description

BLOCK	NAME	TYPE	NUM	DESCRIPTION	INTERFACE
General	XTAL1	I	1	40MHz crystal input	3.3V LVTTL
	XTAL2	O	1	40MHz crystal output	–
	NRESET	I	1	General system reset	5V Tolerant LVTTL
	NTEST_MODE	I	1	Reserved	3.3V
	GPIO(8:0)	I/O	9	General purpose IOs	5V Tolerant LVTTL
Serial port	TXD_UART	O	1	Serial port transmit	5V Tolerant LVTTL
	RXD_UART	I	1	Serial port receive	5V Tolerant LVTTL
SPI	SPI _CLOCK	O	1	SPI clock	3.3V
	SPI_OUT	O	1	SPI data out	3.3V
	SPI_IN	I	1	SPI data in	5V Tolerant LVTTL
	SPI_NCS (3:0)	O	4	SPI device chip select	3.3V
Memory	SDRAM_CLOCK	O	1	160MHz SDRAM clock	3.3V
	SDRAM_CLK_FB	I	1	160MHz clock feedback. Connected to SDRAM_CLOCK.	3.3V LVTTL
	NCS_FLASH	O	1	FLASH memory chip select	3.3V
	NOE_FLASH	O	1	FLASH memory output enable	3.3V
	SDRAM_NCS	O	1	SDRAM chip select	3.3V
	NRAS	O	1	SDRAM row access strobe	3.3V
	NCAS	O	1	SDRAM column access strobe	3.3V
	NWE	O		Memory write enable	3.3V
	BA(1:0)	O	2	Bank address select	3.3V
	ADDR(11:0)	O	12	Memory address bus	3.3V
	DQ(15:0)	I/O	16	Memory data bus	3.3V LVTTL
	DQM(H,L)	O	2	SDRAM data mask	3.3V
ADC/DAC	IREF_DAC	I	1	DAC current reference	Analog
	TXP_DAC	O	1	DAC transmission. Positive differential signal.	Analog
	TXM_DAC	O	1	DAC transmission. Negative differential signal.	Analog
	VBG_DAC_ADC	I	1	DAC/ADC band gap reference voltage	Analog
	REFP_ADC	I	1	ADC reference. Add capacitor to V_{SS}.	Analog
	REFM_ADC	I	1	ADC reference. Add capacitor to V_{SS}.	Analog
	VCM_ADC	I	1	Add capacitor to V_{SS}.	Analog
	RXP_ADC	I	1	ADC reception. Positive differential signal.	Analog
	RXM_ADC	I	1	ADC reception. Negative differential signal.	Analog
	IBEXT_ADC	–	1	Reserved	–
	ADC_CLOCK	–	1	Reserved	3.3V
	DAC_CLOCK	–	1	Reserved	3.3V

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BLOCK	NAME	TYPE	NUM	DESCRIPTION	INTERFACE
MII	RXD(3:0)	I	4	Receive data signals	3.3V LVTTL
	RX_ER	I	1	Receive error	3.3V LVTTL
	RX_DV	I	1	Receive data valid	3.3V LVTTL
	RX_CLK	I	1	Receive clock	3.3V LVTTL
	TXD(3:0)	O	4	Transmit data signals	3.3V
	TX_EN	O	1	Transmit enable	3.3V
	TX_CLK	I/O	1	Transmit clock	3.3V LVTTL
	MDC	O	1	Management interface clock	3.3V
	MDIO	I/O	1	Management interface input/output	3.3V LVTTL
JTAG	JTAG_TMS	I	1	Mode select	5V Tolerant LVTTL
	JTAG_TCK	I	1	JTAG clock	5V Tolerant LVTTL
	JTAG_TDI	I	1	Transmit data in	5V Tolerant LVTTL
	JTAG_TDO	O	1	Transmit data out	3.3V
	JTAG_BUSY	O	1	JTAG busy	3.3V
Power	V_{IO}	I	12	Digital V_{CC} IO power	3.3V Power
	V_{CORE}	I	11	Digital V_{CC} core power	1.8V Power
	V_{IO_ANL}	I	7	Analog V_{CC} IO power	3.3V Power
	V_{CORE_ANL}	I	3	Analog V_{CC} core power	1.8V Power
	V_{SS}	I	70	GND	0V

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13 Pinout

BALL	SIGNAL
A1	RXM_ADC
A2	VCM_ADC
A3	RXP_ADC
A4	REFP_ADC
A5	TX_EN
A6	TXD(1)
A7	TXD(3)
A8	NOT CONNECT
A9	NOT CONNECT
A10	RXD(0)
A11	RXD(2)
A12	RX_DV
A13	RX_CLK
A14	MDC
B1	VBG_DAC_ADC
B2	V_{IO_ANL}
B3	V_{IO_ANL}
B4	REFM_ADC
B5	TX_CLK
B6	TXD(0)
B7	TXD(2)
B8	NOT CONNECT
B9	NOT CONNECT
B10	RXD(1)
B11	RXD(3)
B12	RX_ER
B13	MDIO
B14	DQ(1)
C1	IBEXT_ADC
C2	V_{IO_ANL}
C3	V_{SS}
C4	V_{SS}
C5	V_{IO_A}
C6	V_{S}
C7	V_{IO_ANL}
C8	V_{SS}
C9	V_{IO}
C10	V_{SS}
C11	V_{IO}
C12	V_{SS}
C13	DQ(0)
C14	DQ(2)

BALL	SIGNAL
D8	V_{CORE}
D9	V_{SS}
D10	V_{CORE}
D11	V_{SS}
D12	V_{IO}
D13	DQ(3)
D14	DQ(4)
E1	XTAL1
E2	V_{SS}
E3	V_{IO_ANL}
E4	V_{SS}
E5	V_{SS}
E6	V_{SS}
E7	V_{SS}
E8	V_{SS}
E9	V_{SS}
E10	V_{SS}
E11	V_{CORE}
E12	V_{SS}
E13	DQ(5)
E14	DQ(6)
F1	TXM_DAC
F2	DAC_CL[illegible]K
F3	V_{SS}
F4	$V_{COR[illegible]ANL}$
F5	V_{SS}
F6	V_{SS}
F7	V_{SS}
F8	V_{SS}
F9	V_{SS}
F10	V_{SS}
F11	V_{SS}
F12	V_{IO}
F13	DQ(7)
F14	DQ(8)
G1	TXP_DAC
G2	IREF_DAC
G3	V_{IO_ANL}
G4	V_{SS}
G5	V_{SS}
G6	V_{SS}
G7	V_{SS}

BALL	SIGNAL
H1	SPI_CLOCK
H2	SPI_NCS(0)
H3	V_{SS}
H4	V_{CORE}
H5	V_{SS}
H6	V_{SS}
H7	V_{SS}
H8	V_{SS}
H9	V_{SS}
H10	V_{SS}
H11	V_{SS}
H12	V_{IO}
H13	DQ(12)
H14	DQ[illegible]
J1	SPI_N[illegible](1)
J2	SPI_NC[illegible](2)
J3	V_{IO}
J[illegible]	V_{SS}
J5	V_{SS}
J[illegible]	V_{SS}
J7	V_{SS}
J8	V_{SS}
J9	V_{SS}
J10	V_{SS}
J11	V_{CORE}
J12	V_{SS}
J13	DQ(14)
J14	DQ(13)
K1	SPI_NCS(3)
K2	SPI_OUT
K3	V_{SS}
K4	V_{CORE}
K5	V_{SS}
K6	V_{SS}
K7	V_{SS}
K8	V_{SS}
K9	V_{SS}
K10	V_{SS}
K11	V_{SS}
K12	V_{IO}
K13	DQM(H)
K14	DQ(15)

BALL	SIGNAL
L8	V_{SS}
L9	V_{CORE}
L10	V_{SS}
L11	V_{CORE}
L12	V_{SS}
L13	N[illegible]AS
L14	D[illegible]M(L)
M1	NTE[illegible]ST_MODE
M2	TXD_UART
M[illegible]	V_{SS}
M4	V_{IO}
M5	V_{SS}
M6	V_{IO}
M7	V_{SS}
M8	V_{IO}
M9	V_{SS}
M10	V_{IO}
M11	V_{SS}
M12	BA(0)
M13	SDRAM_NCS
M14	NCAS
N1	RXD_UART
N2	GPIO(7)
N3	GPIO(5)
N4	GPIO(3)
N5	GPIO(1)
N6	SDRAM_CLOCK_FB
N7	ADDR(11)
N8	ADDR(8)
N9	ADDR(6)
N10	ADDR(4)
N11	ADDR(2)
N12	ADDR(0)
N13	NOE_FLASH
N14	NWE
P1	GPIO(8)
P2	GPIO(6)
P3	GPIO(4)
P4	GPIO(2)
P5	GPIO(0)
P6	SDRAM_CLOCK
P7	ADDR(10)

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BALL	SIGNAL
D1	XTAL2
D2	ADC_CLOCK
D3	V_{SS}
D4	V_{CORE_ANL}
D5	V_{SS}
D6	V_{CORE_ANL}
D7	V_{SS}

BALL	SIGNAL
G8	V_{SS}
G9	V_{SS}
G10	V_{SS}
G11	V_{CORE}
G12	V_{SS}
G13	DQ(9)
G14	DQ(10)

BALL	SIGNAL
L1	SPI_IN
L2	NRESET
L3	V_{IO}
L4	V_{SS}
L5	V_{CORE}
L6	V_{SS}
L7	V_{CORE}

BALL	SIGNAL
P8	ADDR(9)
P9	ADDR(7)
P10	ADDR(5)
P11	ADDR(3)
P12	ADDR(1)
P13	BA(1)
P14	NCS_FLASH

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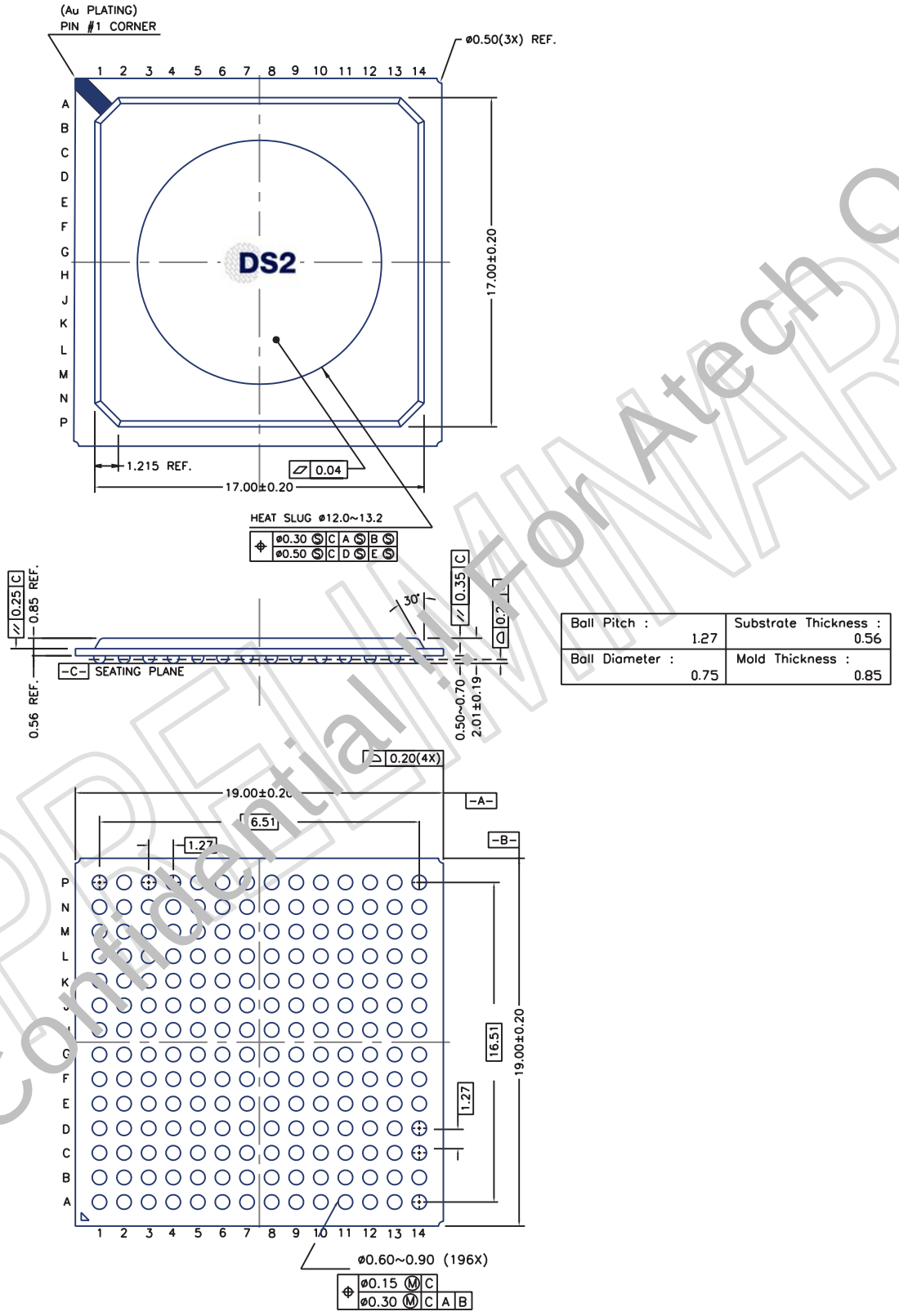
14 Package Outline

Figure 12: HSBGA196



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